IWES 2016

1st Italian Workshop on Embedded Systems

Pisa -- 19 September 2016

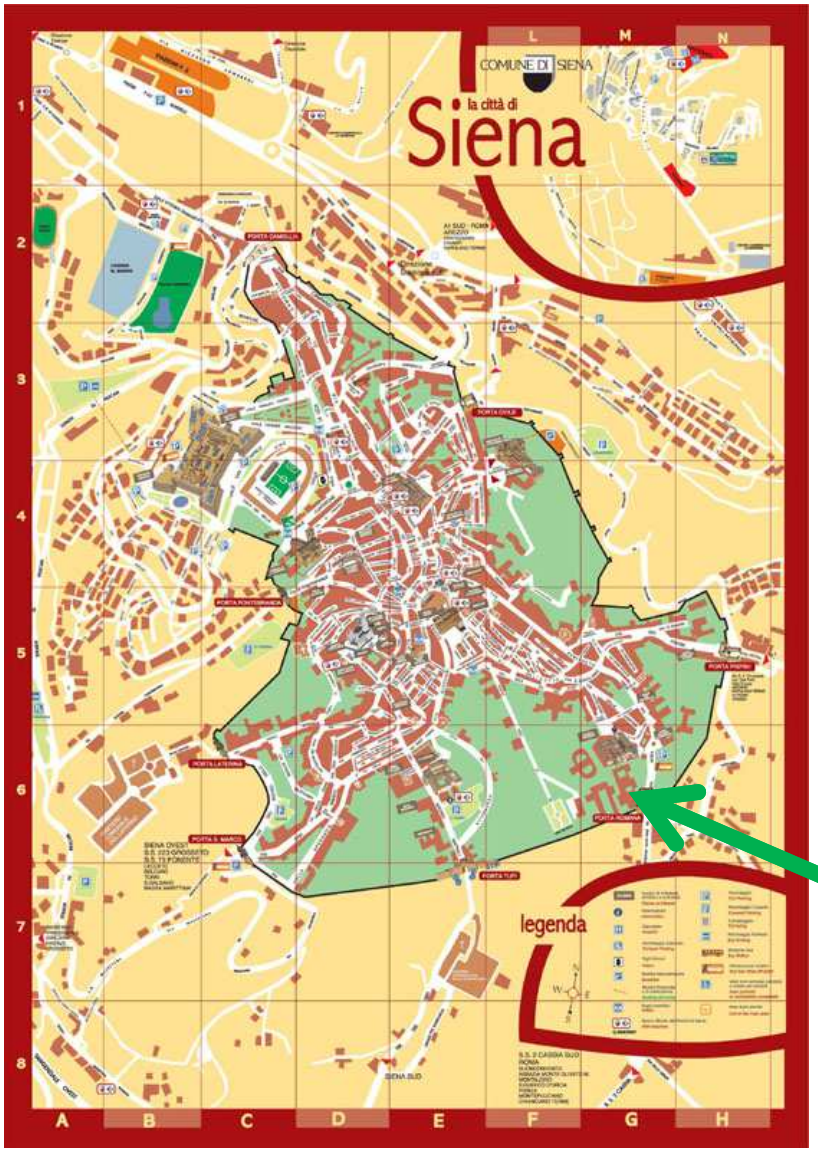
Research Group Overview

Roberto Giorgi
University of Siena, Italy

http://www.dii.unisi.it/~giorgi


Milano
Bergamo
Verona
Venezia
Treviso
Trieste
Padova
Pavia
Torino
Asti
Parma
Modena
Bologna
Ravenna
Genova
Savona
La Spezia
Cesena
Rimini
San Marino
Pisa
Firenze
Livorno
Nizza
Ancona
Arezzo
Siena
Italia
San Benedetto del Tronto
Grosseto
Ascoli Piceno
Terni
Pescara
Chieti
Vasto
Bastia
Parc Naturel Régional de Corse
Corsica
Ajaccio
Porto Vecchio
Roma
Fiumicino
Frosinone
Latina
Foggia
Andria
Napoli
Salerno
Potenza
Pompei
Olbia
Stintino
Sassari
Alghero
Mare Adriatico
Croazia
Fiume
Parenzo
Rovigno
Pola
Zara
Sibenico
Spalat
Velika Go
Varese
Como
E70
E45
E35
E612
E717
E76
E65
E71
E842

Engineering Faculty in Siena



~2km

Our venue

Computer Architecture Lab

Research Group @ UNISI

- 1 Associate prof.: Roberto Giorgi
  - 1 Postdoc, 1 PhD Student, 1 Kernel Hacker
  - HR Throughput: 2 Full-Prof., 2 Researchers, 9 Postdocs, 6 PhD students ---- during the last 7 years
- Courses by me:
  - Bachelor (L1): **Computer Architecture** (6 credits) -3rd year (Italian)
  - Master (L2): **High Performance Computer Architecture** (9 credits) – 1st and 2nd year(English)
- Lab Resources
  - 64-core (x86) CC-NUMA w/1024GiB RAM
  - 48-core+256GiB, about 15 simulation servers (8-core+32GiB)
  - 12 different FPGA boards ranging from Virtex-6 to Zynq Ultrascale+ (6-core 64 bits)
  - Xeon Phi, Maxeler Dataflow computer, GPUs, 50+ embedded boards, (20+ workstations)

AXIOM

Agile, eXtensible, fast I/O Module for the cyber-physical era

2015-2017 -- 4Meuro funding

Brief introduction to the AXIOM project

Roberto Giorgi
University of Siena, Italy

University of Siena
(Coordinator Partner)

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

FORTH
Institute of Computer Science

EVIDENCE
EMBEDDING TECHNOLOGY

herta security

SECO

VIMAR
energia positiva

FUTURE AND EMERGING TECHNOLOGIES
6.13 Meuro funding 2010-13

Exploiting Dataflow Parallelism in Teradevice Computing

TERAFLUX

http://teraflux.eu

Università di Siena (Coordinator)

Barcelona Supercomputing Center

INRIA

University of Augsburg

University of Manchester

University of Cyprus

University of Delaware (USA)

Contact: Prof. Roberto Giorgi (project coordinator): http://www.dii.unisi.it/~giorgi

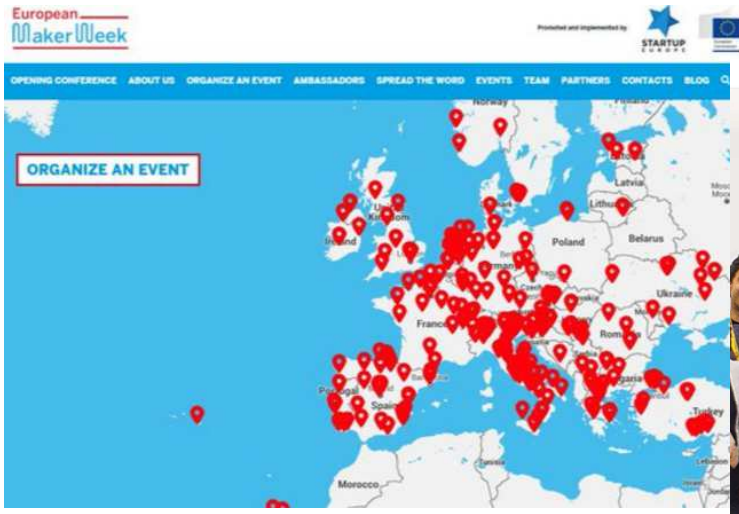
ERA Embedded Reconfigurable Architectures

Project number: 249059

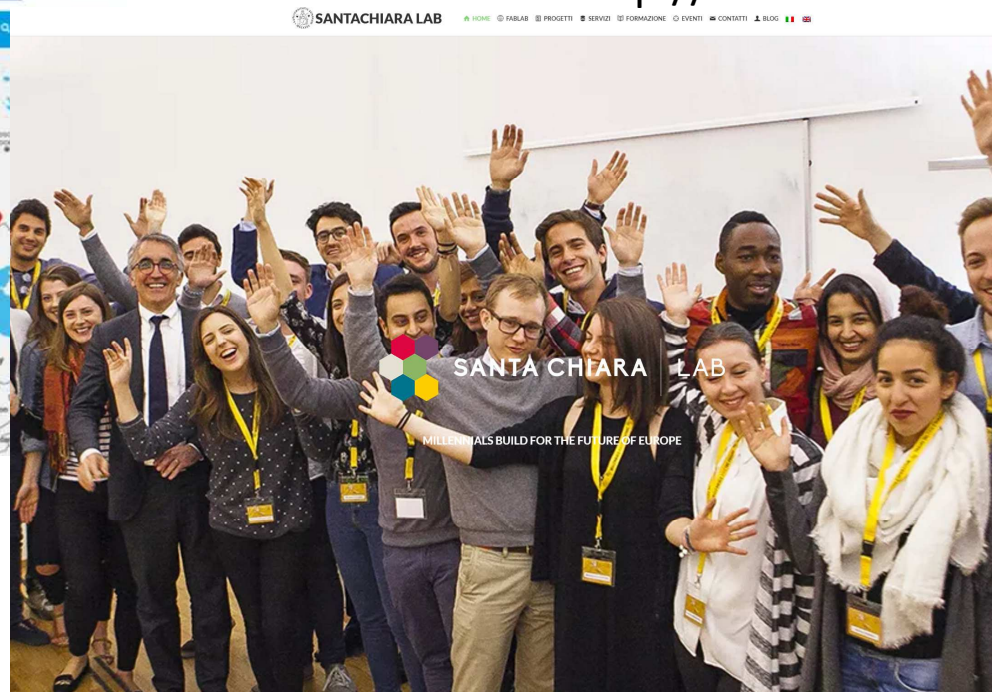
FP7 – 2010-2013 -- ~ 3 Meuro funding

Xilinx Virtex6

Cooperation with SantaChiaraLab (100m from us), Dept. Cognitive Science (in-building) & SECO (Arezzo)



http://santachiaralab.unisi.it/

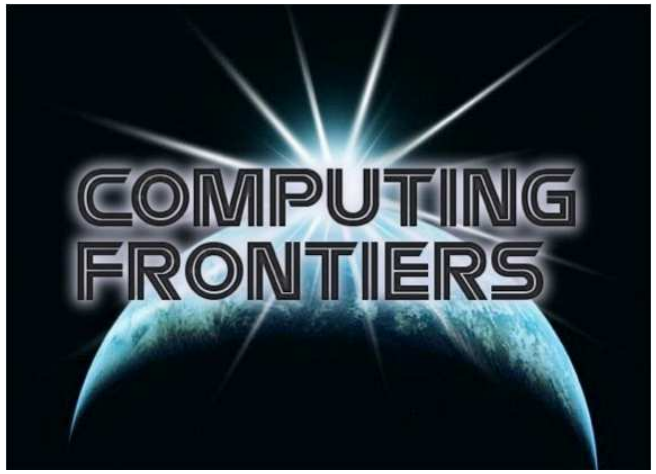


UDOO X86 FOR CLUSTER

SECO/UNISI achievements:

- 2014: UDOO-ARM (99 $ PC+Arduino) → 600k$ on Kickstarter
- 2016: UDOO-x86 (PC+Arduino, 10x faster than Raspberry-3) → 800k$ on Kickstarter

POWERED BY OmpSs
THANKS TO AXIOM



ACM International Conference on Computing Frontiers'17

15-17 May 2017 – Siena, Italy

www.computingfrontiers.org

acm sigmicro

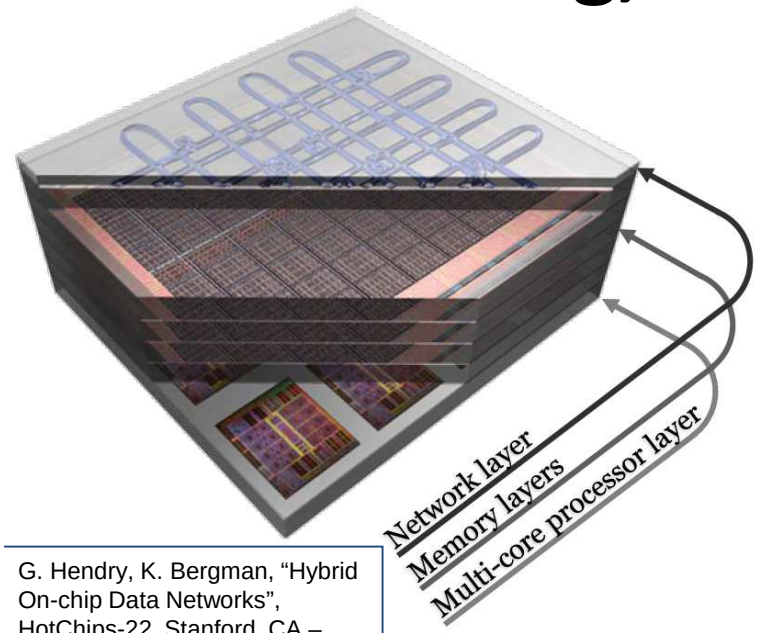
Siena, the city

Siena sorroundings

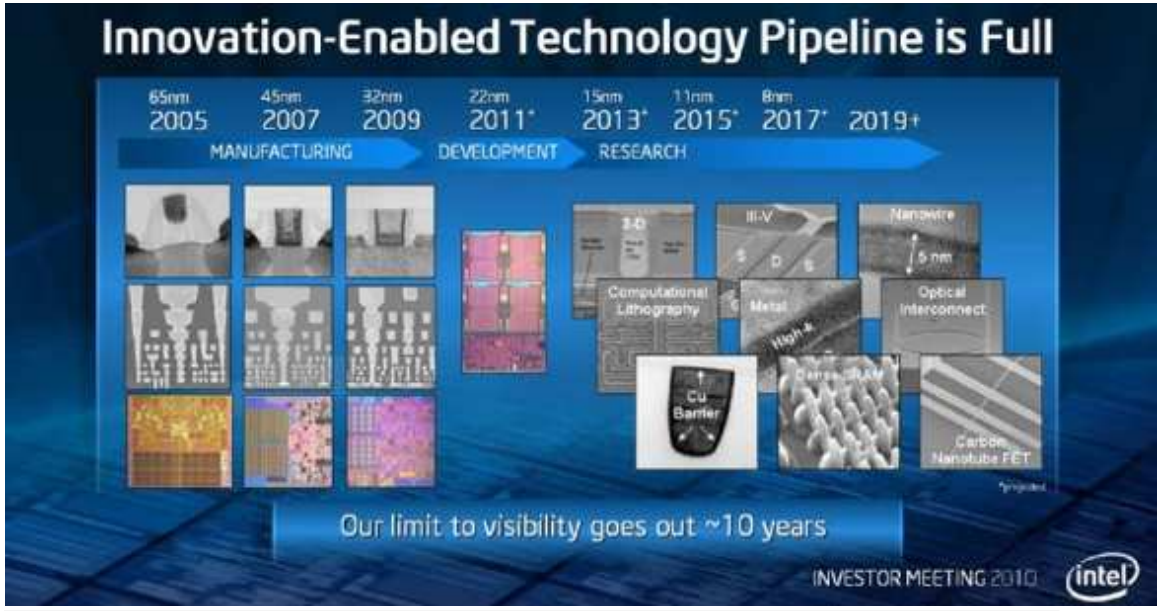
TERAFLUX

(Nearer) Future Scenarios

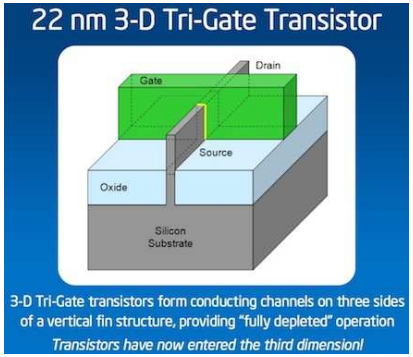
== 3D stacking, 8nm, 3D transistors, Graphene

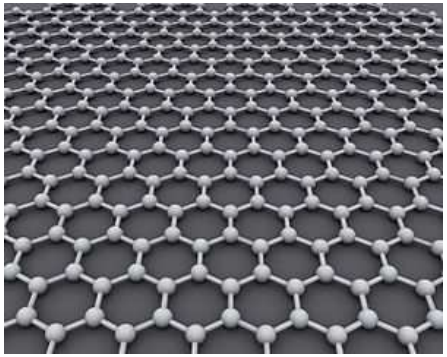


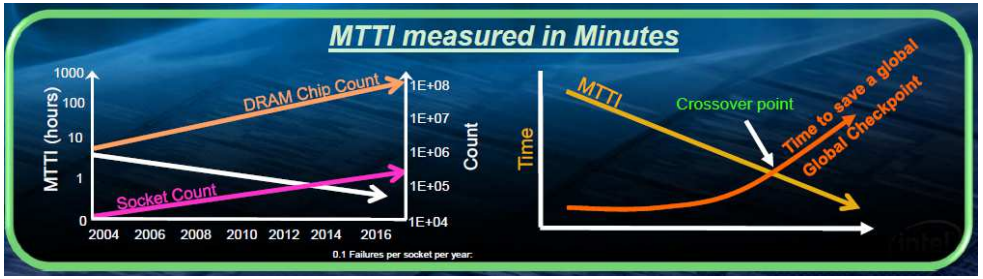
G. Hendry, K. Bergman, "Hybrid On-chip Data Networks", HotChips-22, Stanford, CA – Aug. 2010



Fab D1X (OR), 42 (AZ), 24 (Ireland) starting the 14nm node in 2013







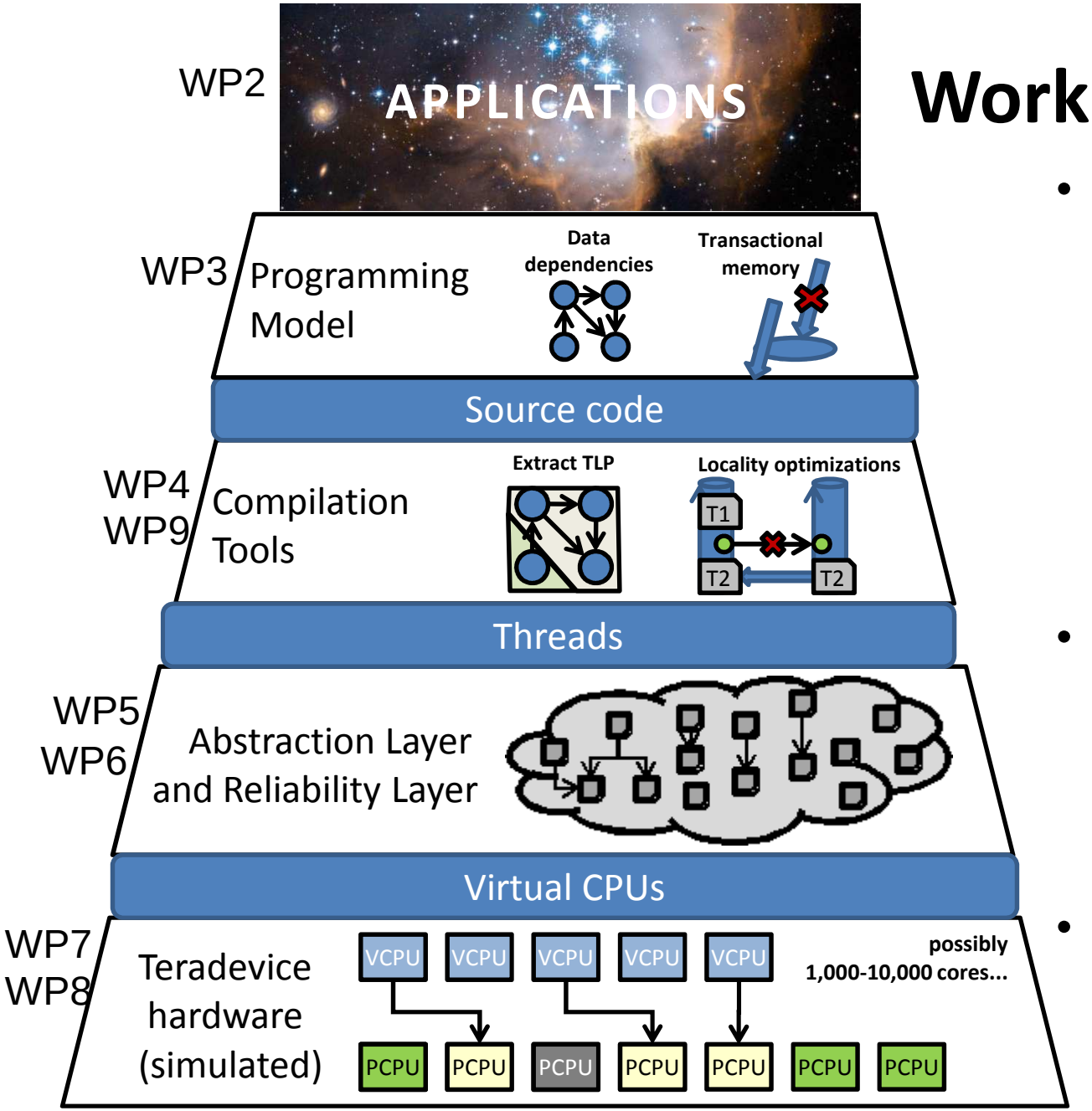
Pawloski, May 2011, Exascale Seminar, Ghent

DATAFLOW

A Scheme of Computation in which an activity is initiated by presence of the data it needs to perform its function

(Jack Dennis)

Working Hypothesis

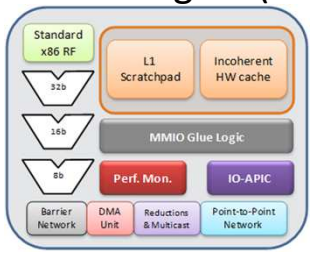


- 1000 Billion- or 1 TERA-device computing platforms pose new challenges:
  - (at least) programmability, complexity of design, reliability
- TERAFLUX context:
  - High performance computing and applications (not necessarily embedded)
- TERAFLUX scope:
  - Exploiting a less exploited path (DATAFLOW) at each level of abstraction

UD's Involvement in Exascale Computing

Traleika Glacier: System Architecture – X-STACK project

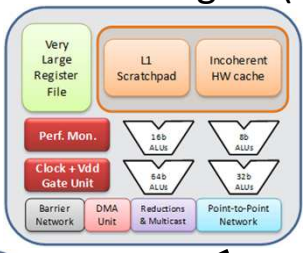
Control Engine (CE)



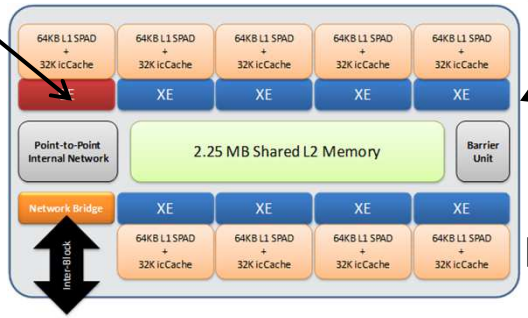
Optimized for execution model and resiliency

Optimized for apps
Large local stores
for data locality

Execution Engine (XE)

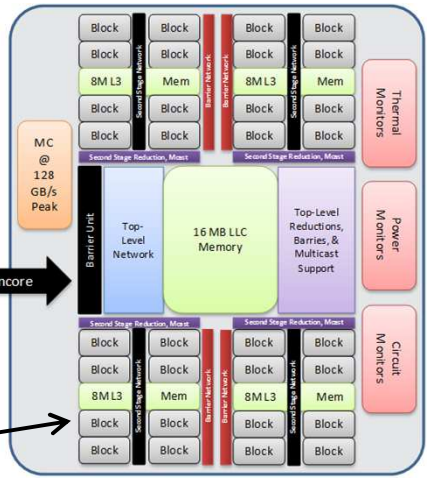


Node



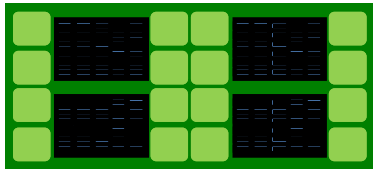
Large local stores (locality)
Sensors for self-awareness
Fine grain energy management

Processor Chip

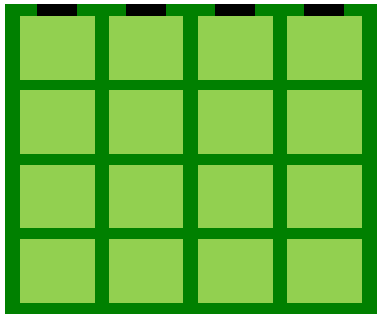


Hierarchical, heterogeneous interconnect

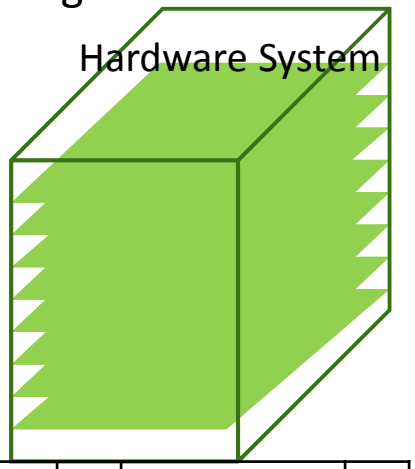
Processor board with DRAM



Cluster



Hardware System



E Efficiency	✓	Scalability	✓	Programmability	✓	Perf Portability		Resiliency	✓

Courtesy of W.Pinfold and S.Borkar, Intel Corp

DF-Threads (DataFlow Threads)

- We built a demonstrator based on HP-Labs COTSon simulator for Dataflow Based execution
- Running 220 instances of 32-core Linux (full-system) virtual machines – 7000+ cores
- We seamleasly run millions of DF-threads (x86 binaries compiled with GCC) with almost linear speed-up on a 1024-core (x86) without need of global cache coherence
- General computation are supported – Transactional Memory is joined to Dataflow to support undeterministic computations with shared state

R. Giorgi, P. Faraboschi, "An Introduction to DF-Threads and their Execution Model", ***IEEE MPP***, Paris, France, Oct. 2014, pp. 60-65.

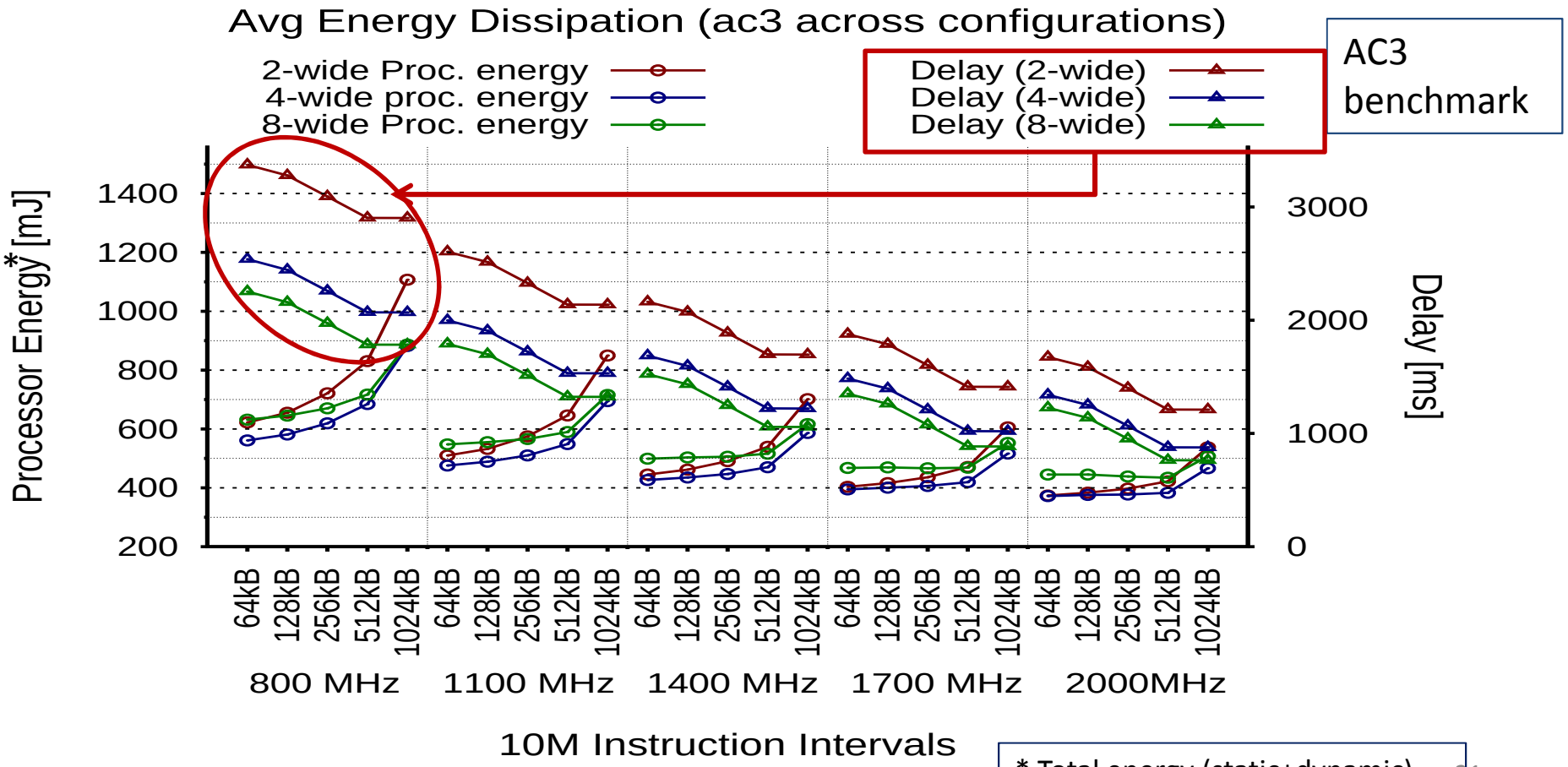
ERA

ERA Target System

- Smartphone with FPGA-based SoCs (e.g Zynq)
- Exploring the energy efficiency of reconfigurable hardware

Benchmarks analysis from energy+delay viewpoint

- **DYNAMYC ENERGY** consumption and **DELAY** while varying L2 cache-size, issue-width, frequency
- Delay significantly decreases with L2 cache size, frequency, issue-width (total energy as in previous slide)
- These behaviors have been confirmed across all the EBS applications



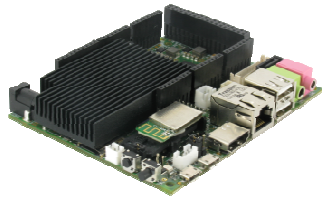
* Total energy (static+dynamic)

AXIOM

AXIOM main goal

- Building a ready-to-market Single Board Computer (SBC) able to address high performance computations in scenarios like
  - Smart Video-surveillance
  - Smart Living & Smart Home

CAN WE DO THAT ?



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UDOO X86 FOR CLUSTER

FIRST PROTOTYPE UNDER REVIEW

- Stackup definition
  - 10 layers PCB
  - HS/LS/power planes arrangement
- Placement
  - Achieve mechanical and electrical constraints
- Routing (WIP)
  - Design for power/signal integrity
- 3D model available