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Simulation Based Formal Verification of Cyber-physical Systems

SyLVaaS: System Level Verification as a Service

Toni Mancini, Annalisa Massini, Federico Mari, Igor Melatti,
Ivano Salvo, Enrico Tronci

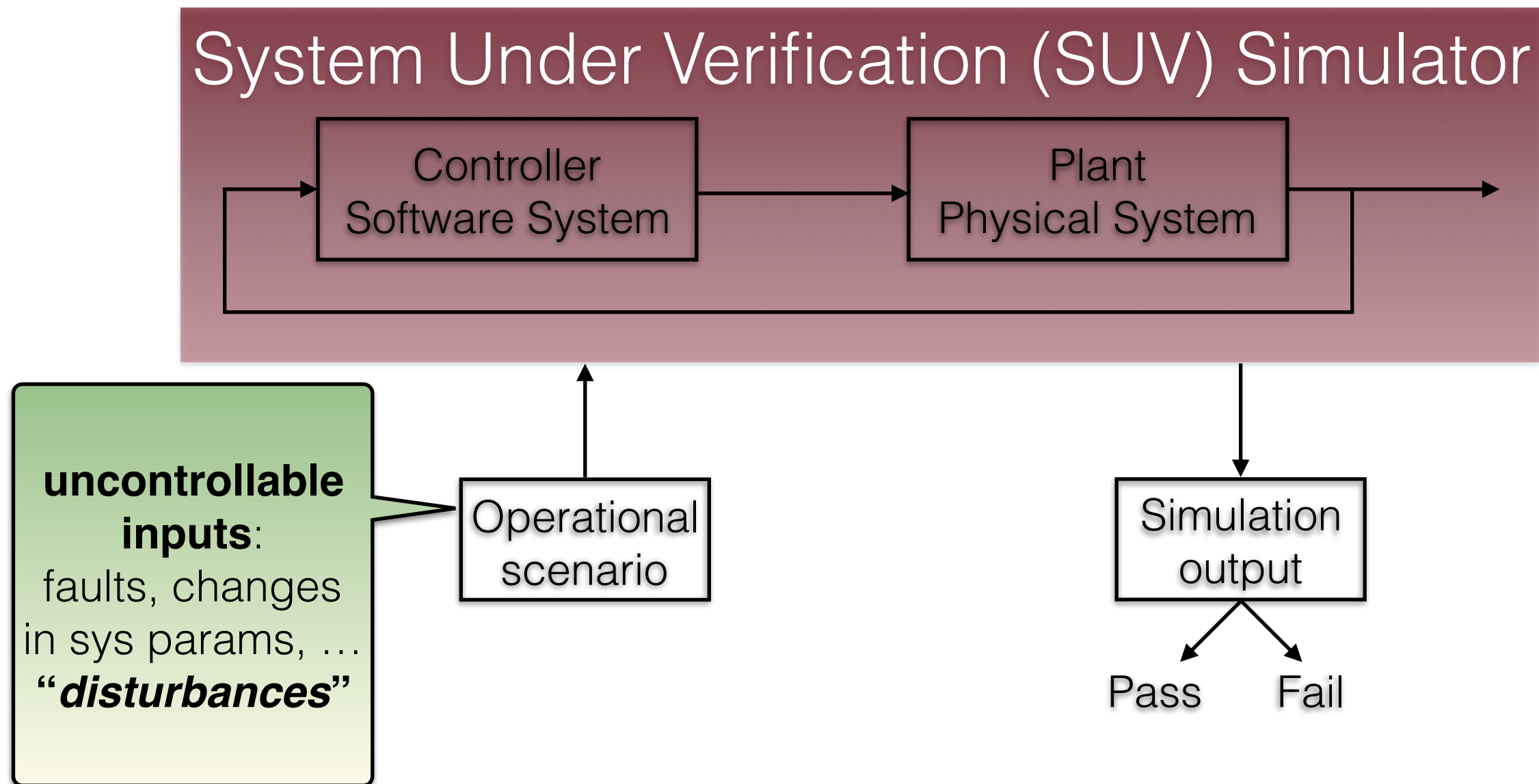
Computer Science Department
Sapienza University of Rome, Italy
<http://mclab.di.uniroma1.it>

System Level Verification of CPSs

- **Cyber Physical System (CPS):** hw + sw components
⇒ Can be modelled as **Hybrid System**
- **System Level Verification (SLV):** to verify that the **whole** system (hw+sw) satisfies given specifications
- CPSs of industrial relevance **too complex** for SLV to be performed by model checkers for Hybrid Systems
- **Main workhorse for SLV:** Hardware in The Loop Simulation

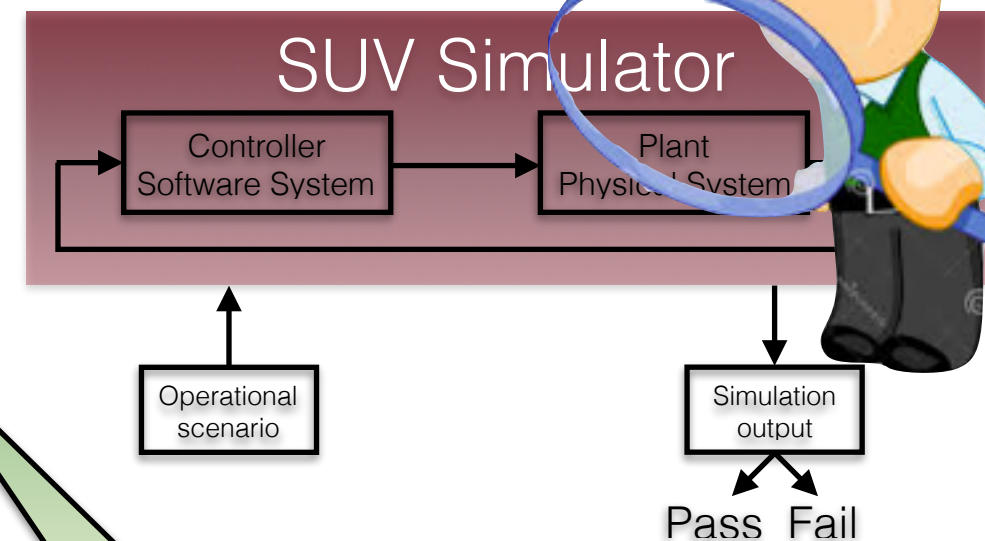
Hardware in The Loop Simulation

- Hardware in The Loop Simulation (HILS): replace hardware with a software simulator
- Supported by Model Based Design Tools as Simulink, VisSim, ...



HILS Campaign: Main Obstacles

- **Effort** needed to define the **operational scenarios** defining disturbances to be injected into the system under verification.
- **Computation time** needed to carry out the simulation campaign itself.
- **Degree of assurance** achieved at the end of the HILS campaign: did we consider **all** relevant operational scenarios?
- **Graceful degradation**: what can we say about the error probability **during** the HILS campaign?



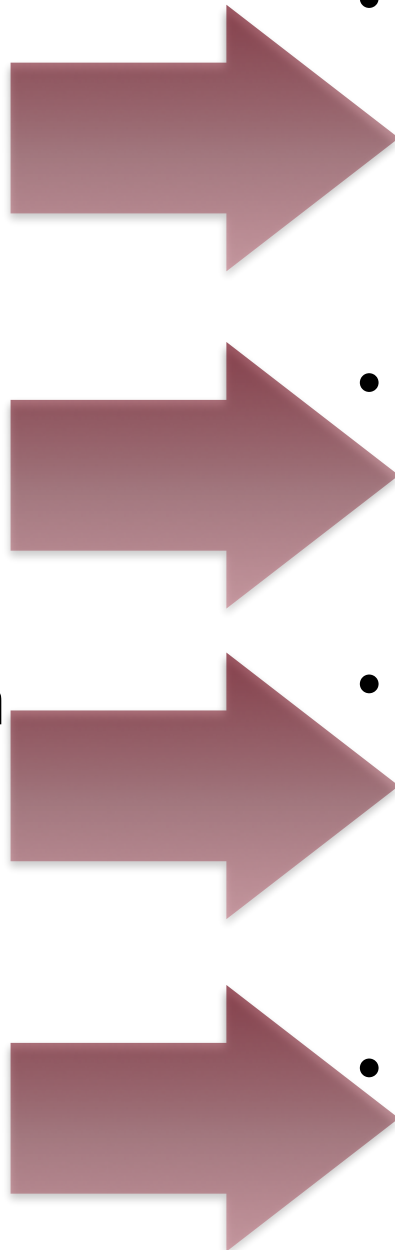
Hard to be done **manually**

Can take **weeks!**

“Did I overlook anything?”

“What can I say if I **abort** verification **now?**”

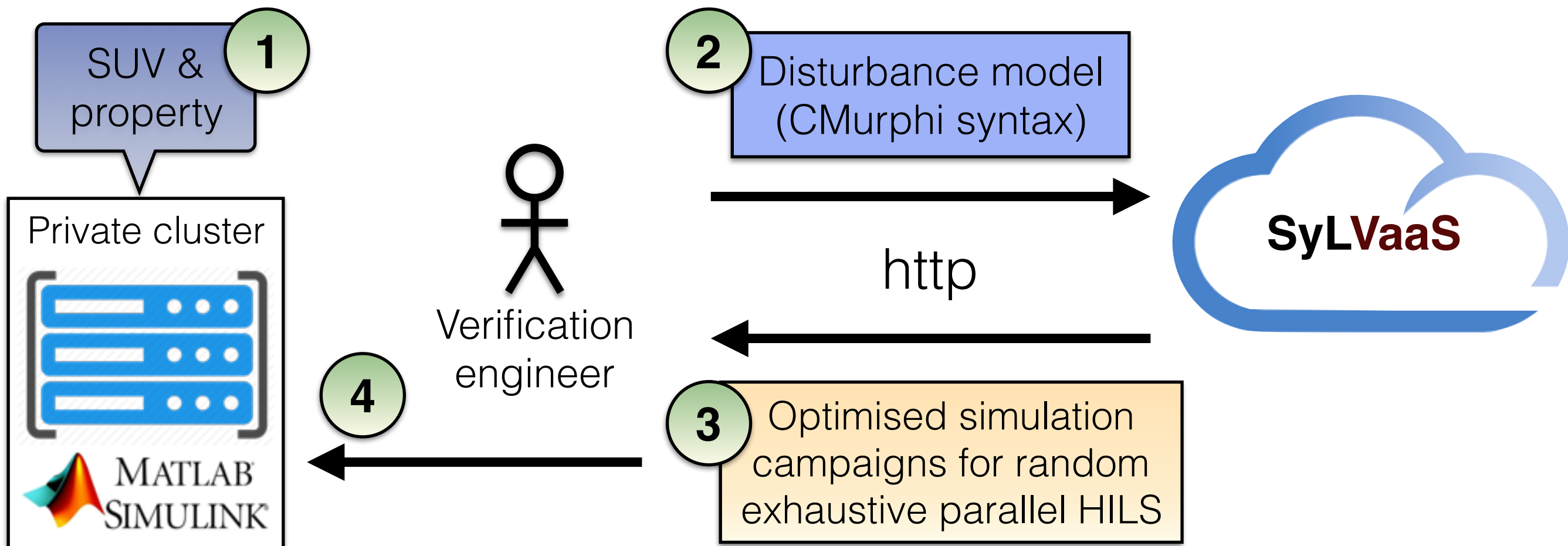
Our approach to System Level Formal Verification

- **Effort** needed to define the **operational scenarios** defining disturbances to be injected into the system under verification.
 - **Degree of assurance**: did we consider **all** relevant operational scenarios?
 - **Graceful degradation**: what can we say about the error probability **during** the HILS campaign?
 - **Computation time** needed to carry out the simulation campaign itself.
- 
- **Formal** model of operational scenarios (**disturbance model**) as a FSA described in a high-level language (CMurphi)
 - **Exhaustive** system level verification wrt operational scenarios defined by the model
 - **Anytime random algorithm**: at any time we compute an **upper bound** to **Omission Probability**
 - **Embarrassing parallel multi-core** approach to speed up simulation + optimisation

[CAV13, PDP14, DSD14, PDP15, Microprocessors & Microsystems 2016, Fundamenta Informaticae 2016]

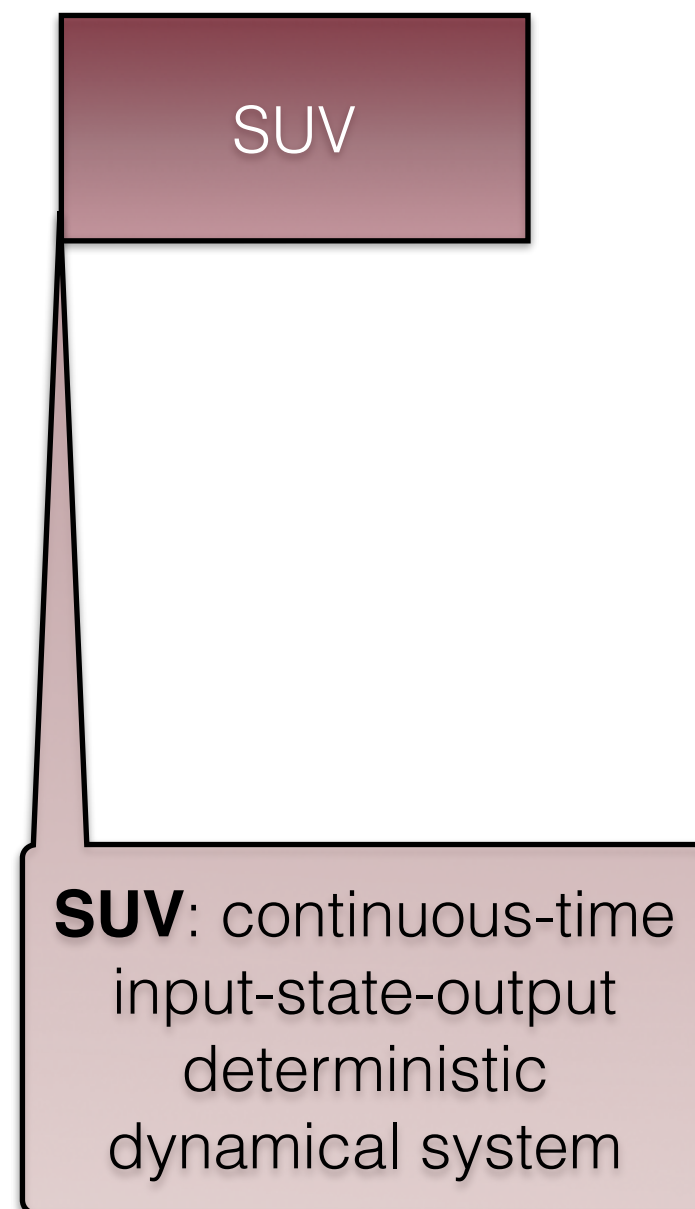
SyLVaaS

- Introduces **Verification as a Service paradigm**
- Supports companies in the CPS design business in their daily verification activities
- Allows keeping both the SUV model and the property to be verified secret (**Intellectual Property protection**)

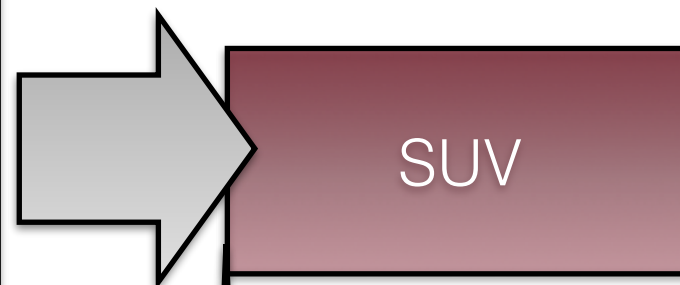
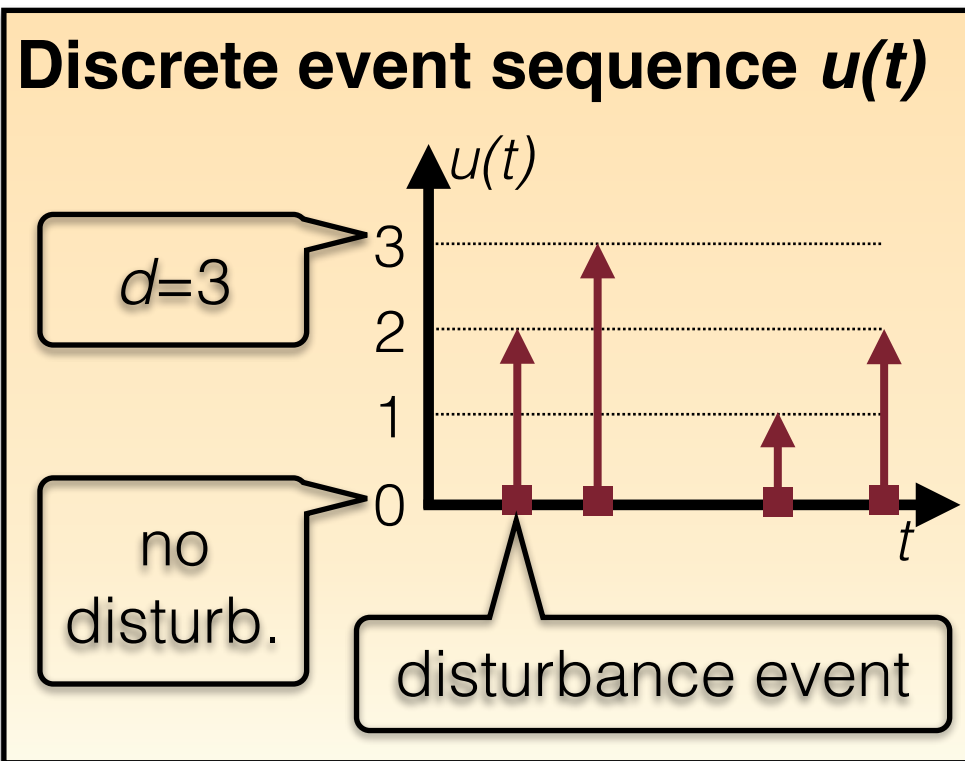


Modelling the Operational Environment

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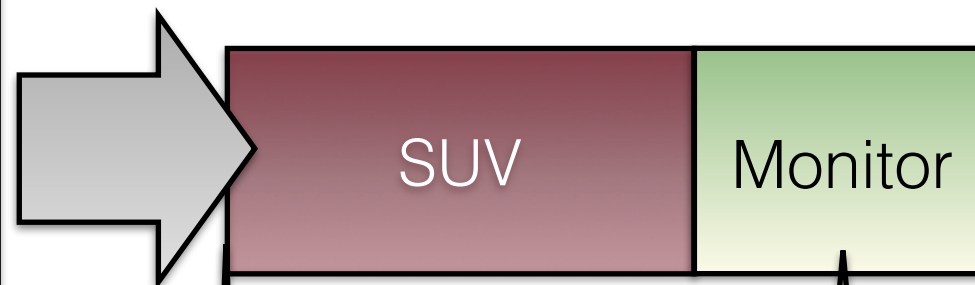
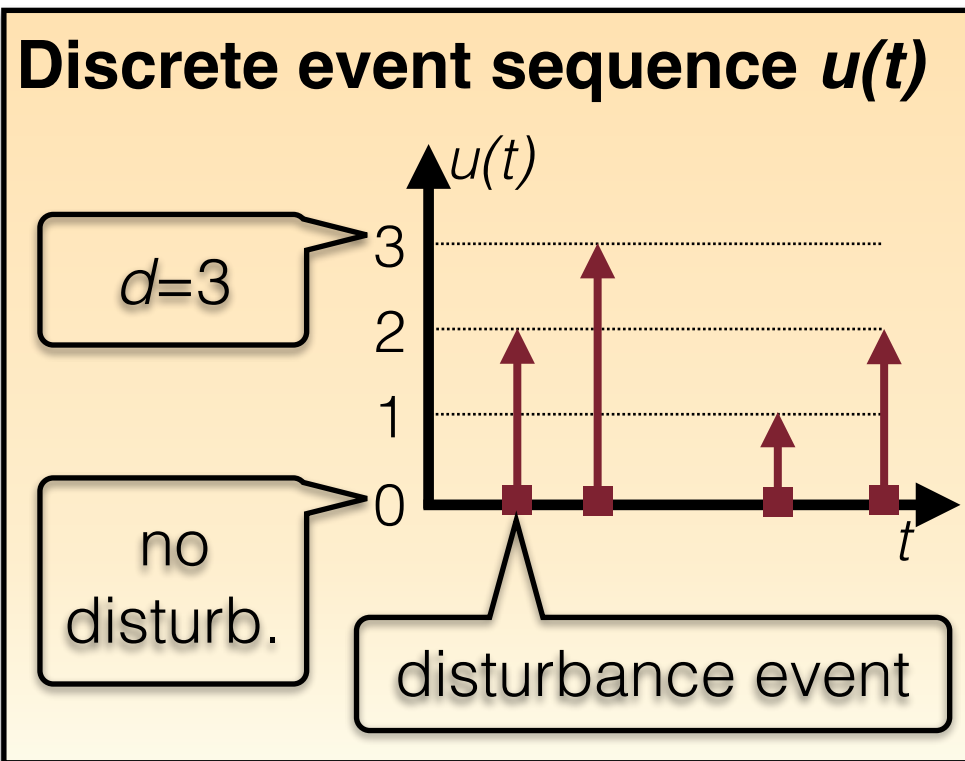
SUV input: discrete event seq.

- Associates to each (real) t a disturbance event within $[0, d]$
- Differs from 0 (no disturbance) in a finite number of time-points

...no system can withstand an infinite number of disturbances within a finite time

SUV: continuous-time
input-state-output
deterministic
dynamical system

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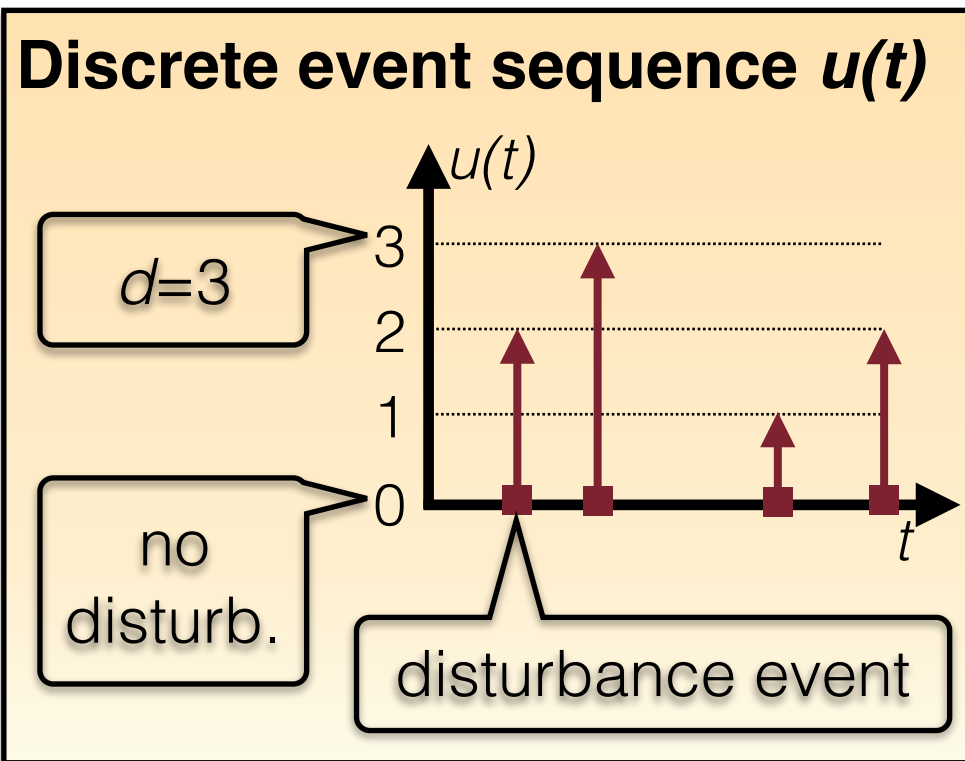
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Property to be verified:

embedded in a continuous-time SUV monitor

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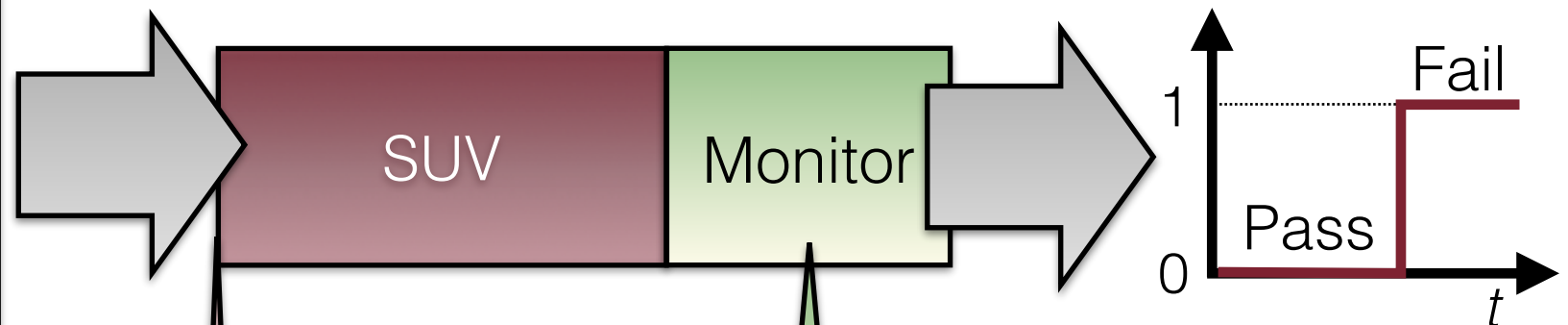
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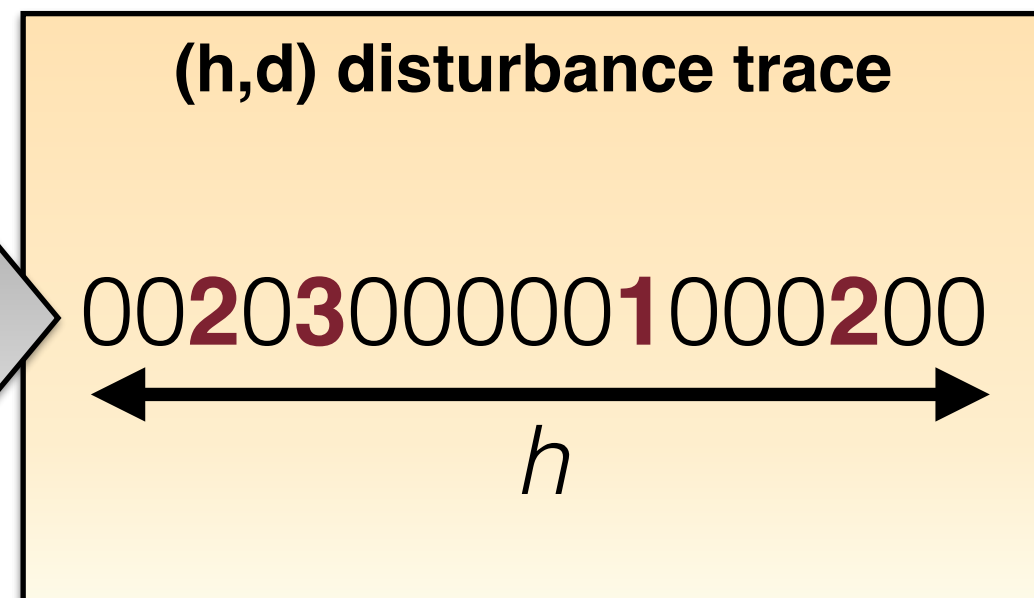
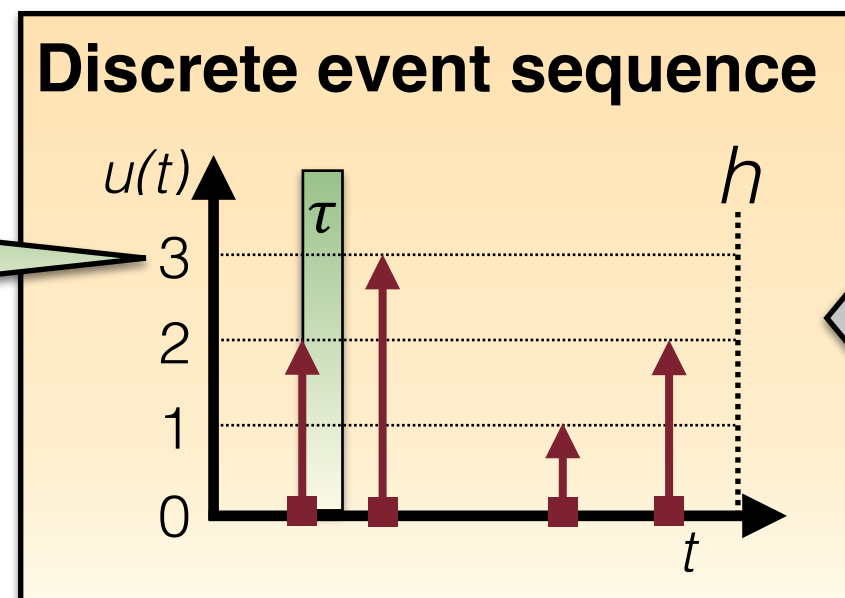
SUV: continuous-time input-state-output deterministic dynamical system

SUV output: 0 at start; goes to and stays 1 as soon as error is detected

Discrete Event Seq's & Disturbance Traces

We aim at **Bounded System Level Formal Verification**:

- Bounded **time horizon**: h
- Bounded **time quantum** between disturbances: τ



Disturbance Model

- Defining all disturbance sequences the SUV should withstand cannot be done manually for large CPSs
- Approach: use high-level modelling language to define disturbance model as a **Finite State Automaton**

A tiny example

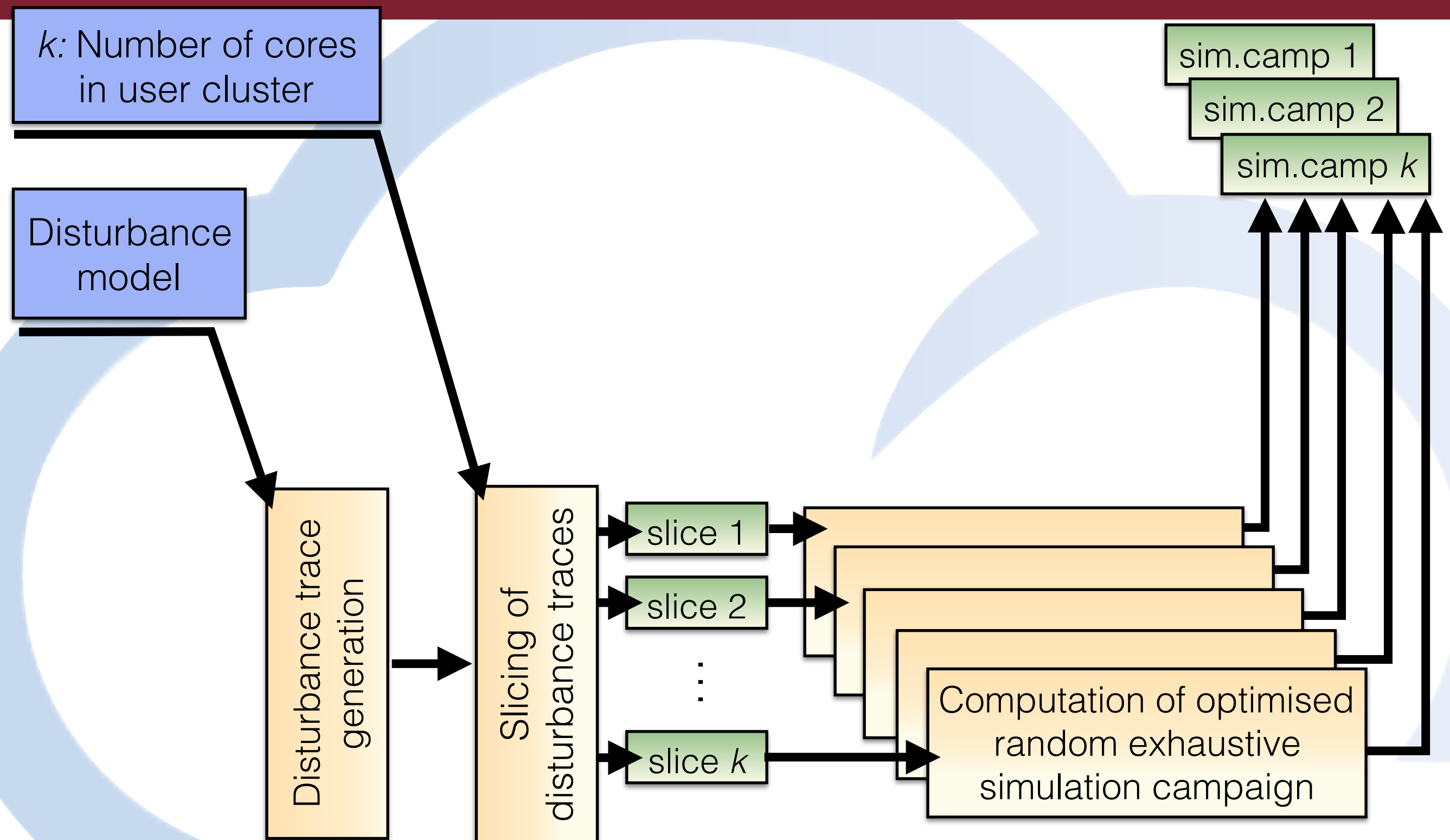
- Just one disturbance (fault), always recovered within 4 seconds
- At least 5 seconds between two consecutive disturbances
- Time quantum $\tau = 1$ second
- Time horizon $h = 6$ seconds

```
function disturbanceModel(h)
  c ← 0; /* counter */
  t ← 0; /* time */
  while t ≤ h do
    d ← read(); t ← t + 1;
    if c > 0 then c ← c - 1;
    if d = 1 then
      if c > 0 then return ⊗;
      else c ← 4;
  return ✓;
end
```

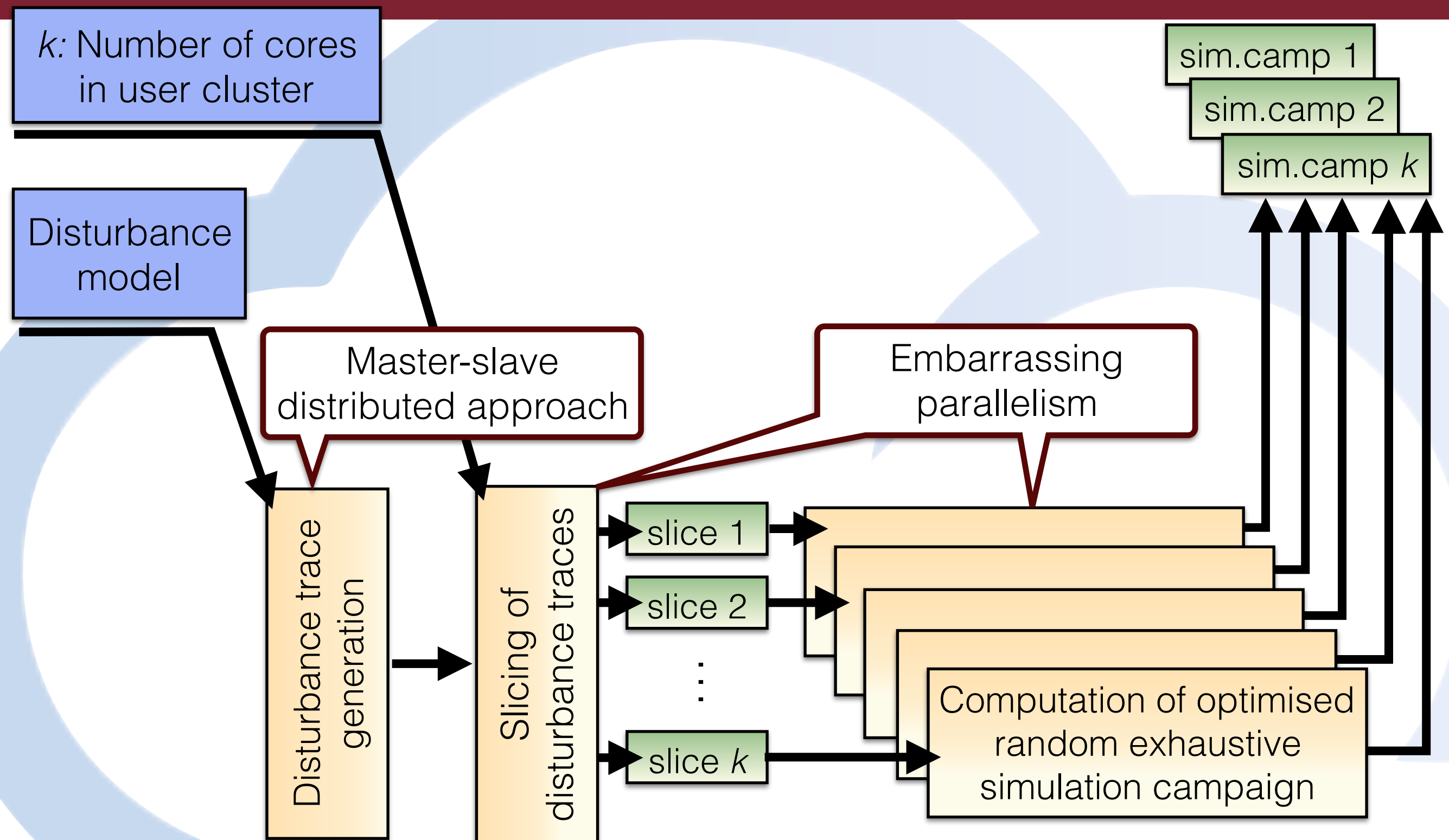
FSA recognising **admissible disturbance traces**
(we actually use the rich language of the
CMurphi model checker)

000000✓ 010000✓ ... overall 8 adm
000001✓ 010001⊗
000010✓ 01001⊗ disturbance traces

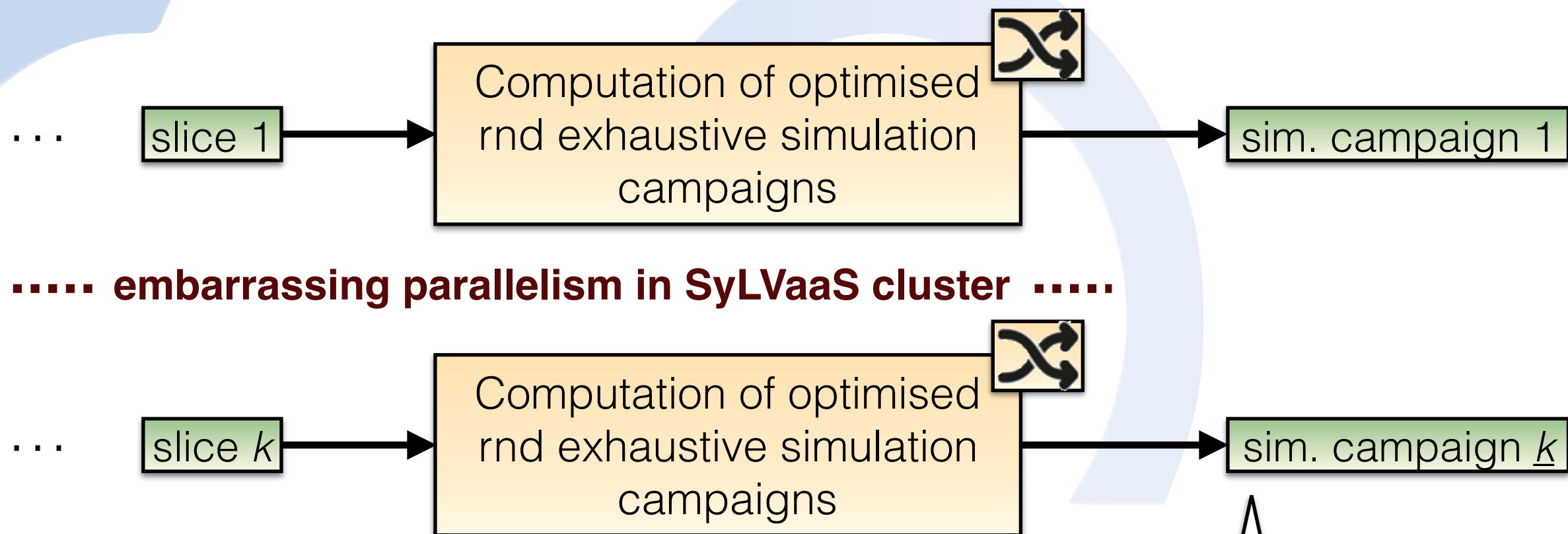
SyLVaaS Workflow



SyLVaaS Workflow



Optimised Rnd Exhaustive Sim. Campaigns



- **Optimisation:** use of load/store commands avoids revisiting previously visited simulation states as much as possible
- **Exhaustiveness:** all disturbance traces in input slice are verified
- **Randomness:** trace verification order is randomised

Sequence of simulator commands:

- **inj_run(*e*, *t*):** inject disturbance and advance simulation
- **store(*l*):** store current sim. state into mass memory
- **load(*l*):** set current sim. state from previously stored state
- **free(*l*):** free stored sim. state stored

Optimised Rnd Exhaustive Sim. Campaigns

Optimised Rnd Exhaustive Sim. Campaigns

Slice	
1	0 2 100 1
2	0 2 2000
3	0 2 20 3 0
4	0 2 3 1 10
5	0 2 3 2 20
6	0 3 00 1 0

Optimised Rnd Exhaustive Sim. Campaigns

Slice	
1	0 2 100 1
2	0 2 2000
3	0 2 20 3 0
4	0 2 3110
5	0 2 3220
6	0 3 00 1 0

Prefix labelling
during generation
(DFS $\rightarrow$ free!)

Slice of **labelled** traces

1	a 0 b 2 c 1d0e0 f 1 g
2	a 0 b 2 c 2h0i0j0 k
3	a 0 b 2 c 2h0i 3 m0n
4	a 0 b 2 c 3p1q1r0 s
5	a 0 b 2 c 3p2v2w0 x
6	a 0 b 3y0z0α 1 β0λ

Labels
univocally
denote trace
prefixes

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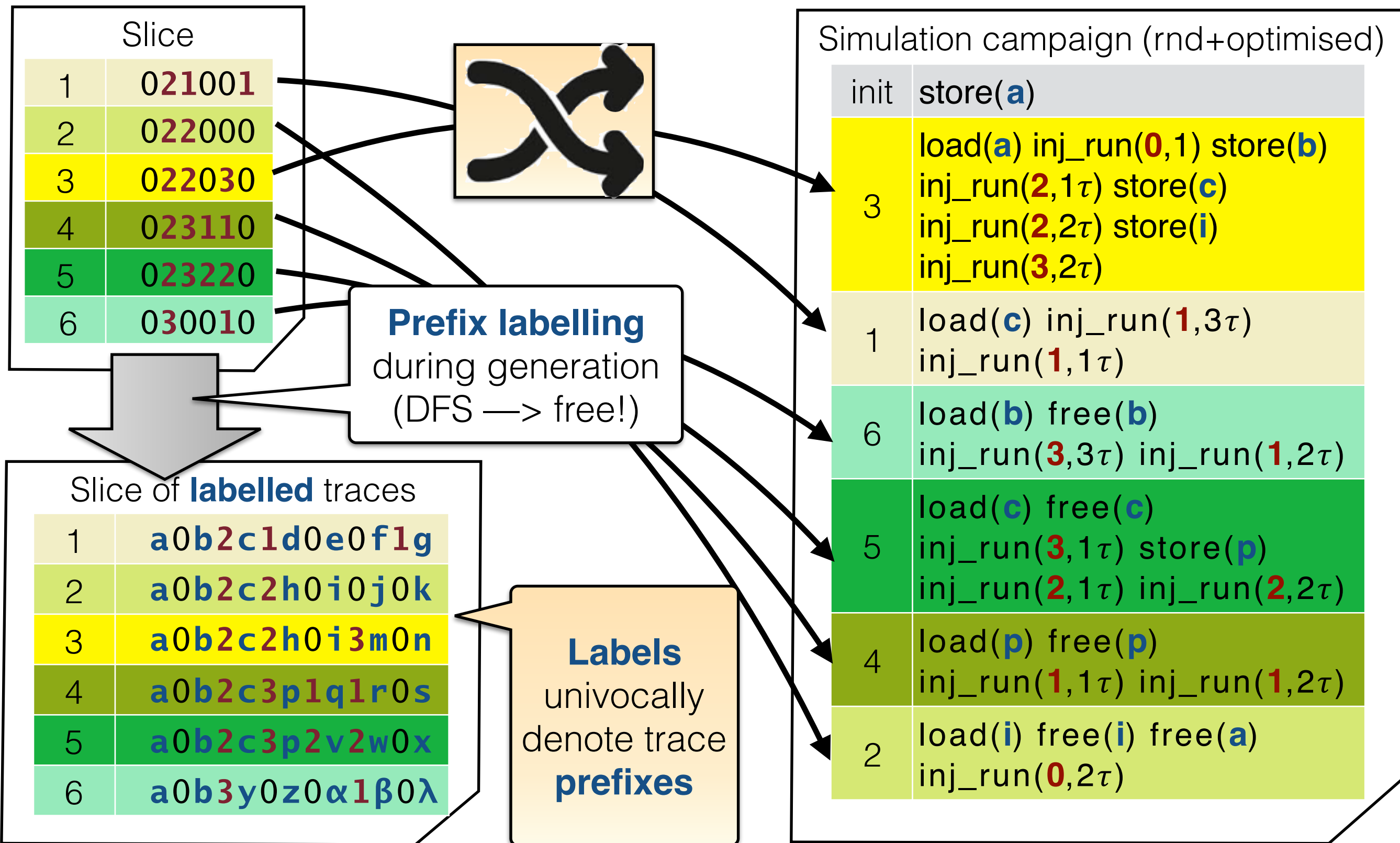
1	a 0 b 2 c 1 d0 e 0 f 1 g
2	a 0 b 2 c 2 h0 i 0 j 0 k
3	a 0 b 2 c 2 h0 i 3 m0 n
4	a 0 b 2 c 3 p 1 q 1 r0 s
5	a 0 b 2 c 3 p 2 v 2 w0 x
6	a 0 b 3 y0z0 α 1 β 0 λ

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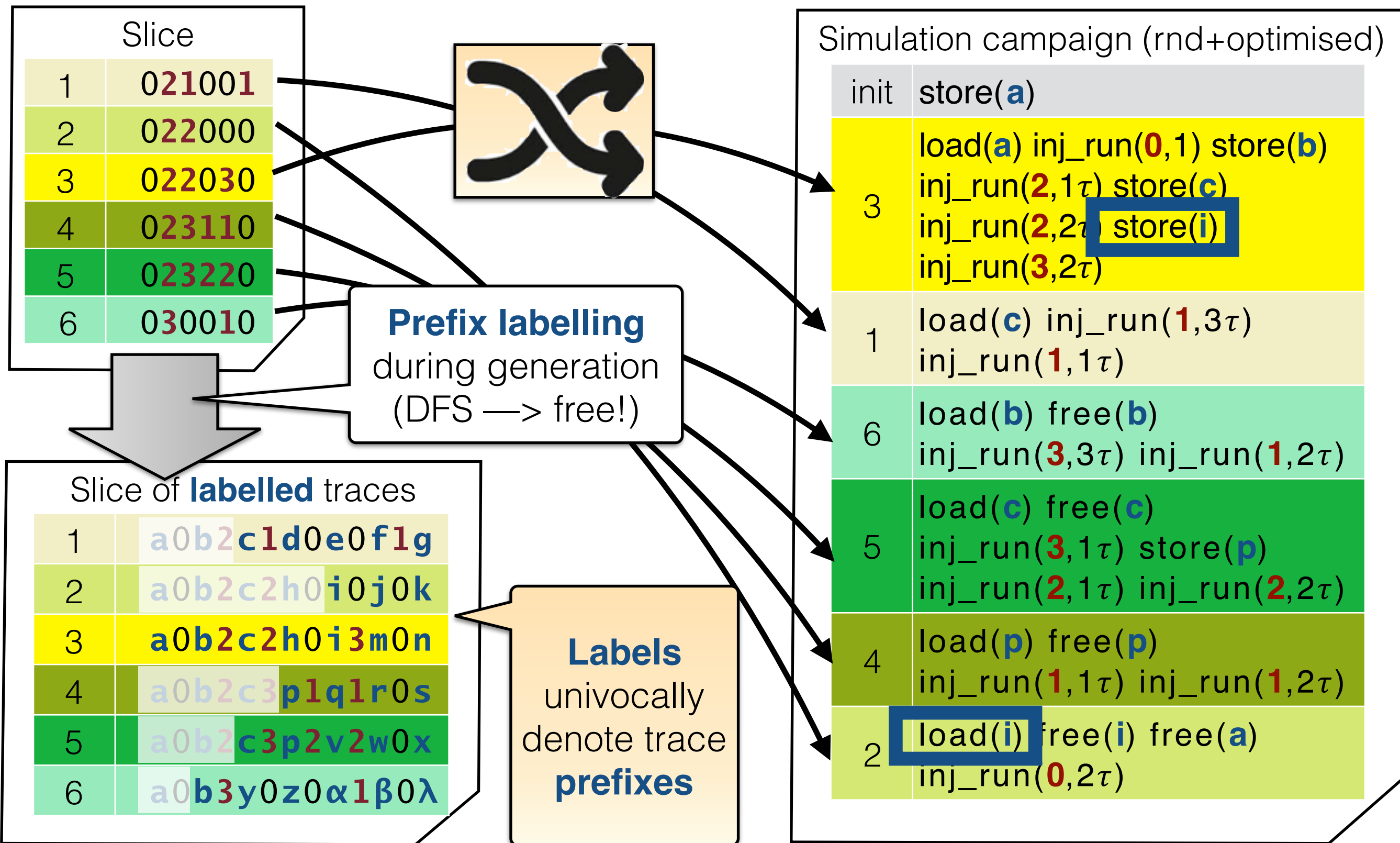
Simulation campaign (rnd+optimised)

init	store(a)
3	load(a) inj_run(0 ,1) store(b) inj_run(2 ,1 τ) store(c) inj_run(2 ,2 τ) store(i) inj_run(3 ,2 τ)
1	load(c) inj_run(1 ,3 τ) inj_run(1 ,1 τ)
6	load(b) free(b) inj_run(3 ,3 τ) inj_run(1 ,2 τ)
5	load(c) free(c) inj_run(3 ,1 τ) store(p) inj_run(2 ,1 τ) inj_run(2 ,2 τ)
4	load(p) free(p) inj_run(1 ,1 τ) inj_run(1 ,2 τ)
2	load(i) free(i) free(a) inj_run(0 ,2 τ)

Optimised Rnd Exhaustive Sim. Campaigns



Optimised Rnd Exhaustive Sim. Campaigns



Embarrassingly Parallel Simulation

Simulation carried out on **user private cluster** (Intellectual Property protection)

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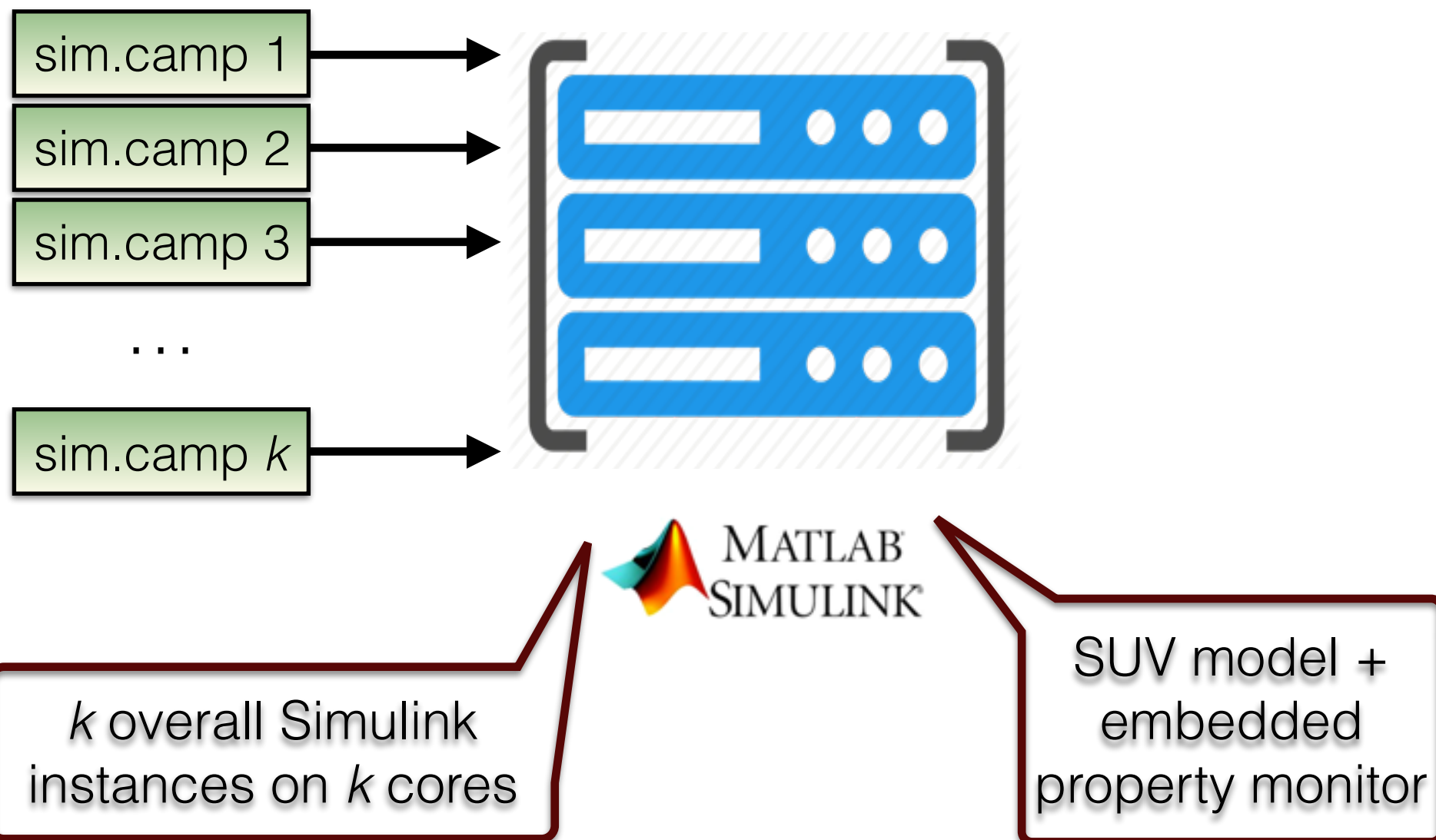


k overall Simulink instances on k cores

SUV model +
embedded
property monitor

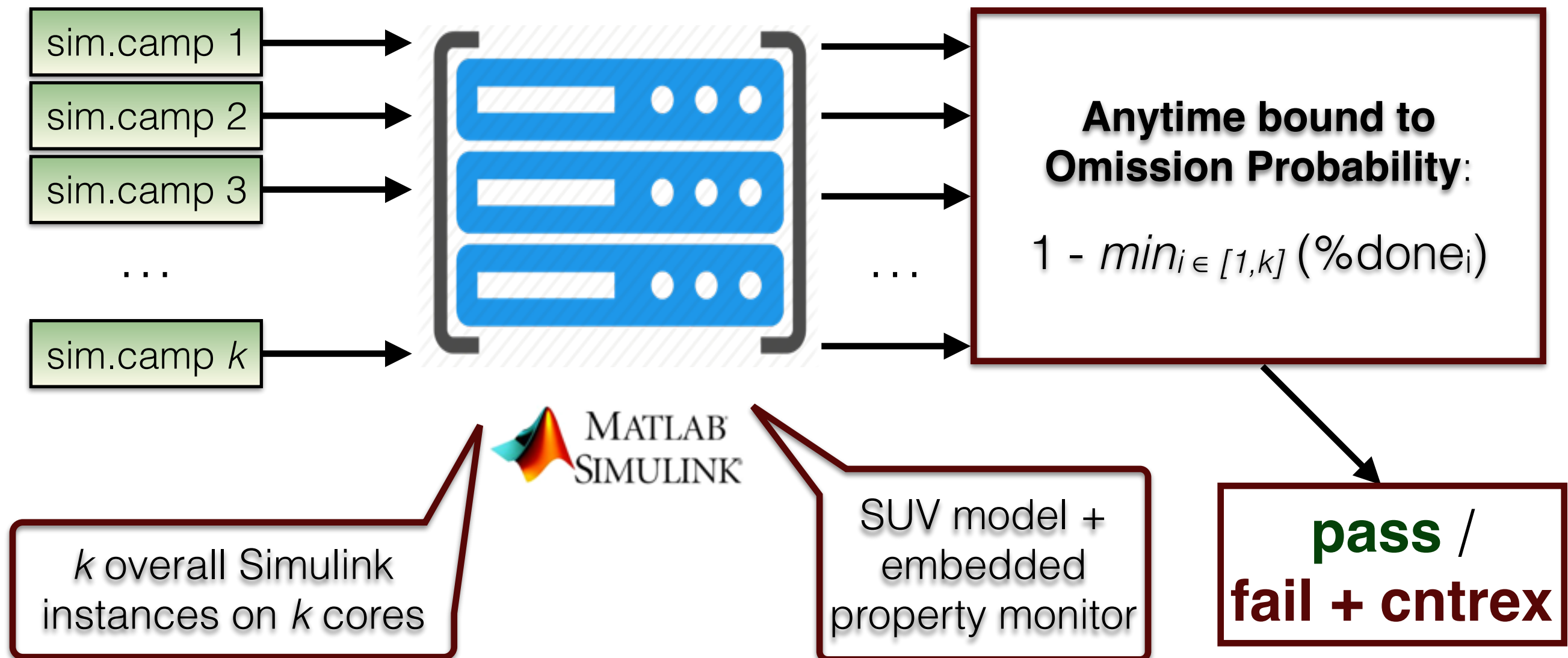
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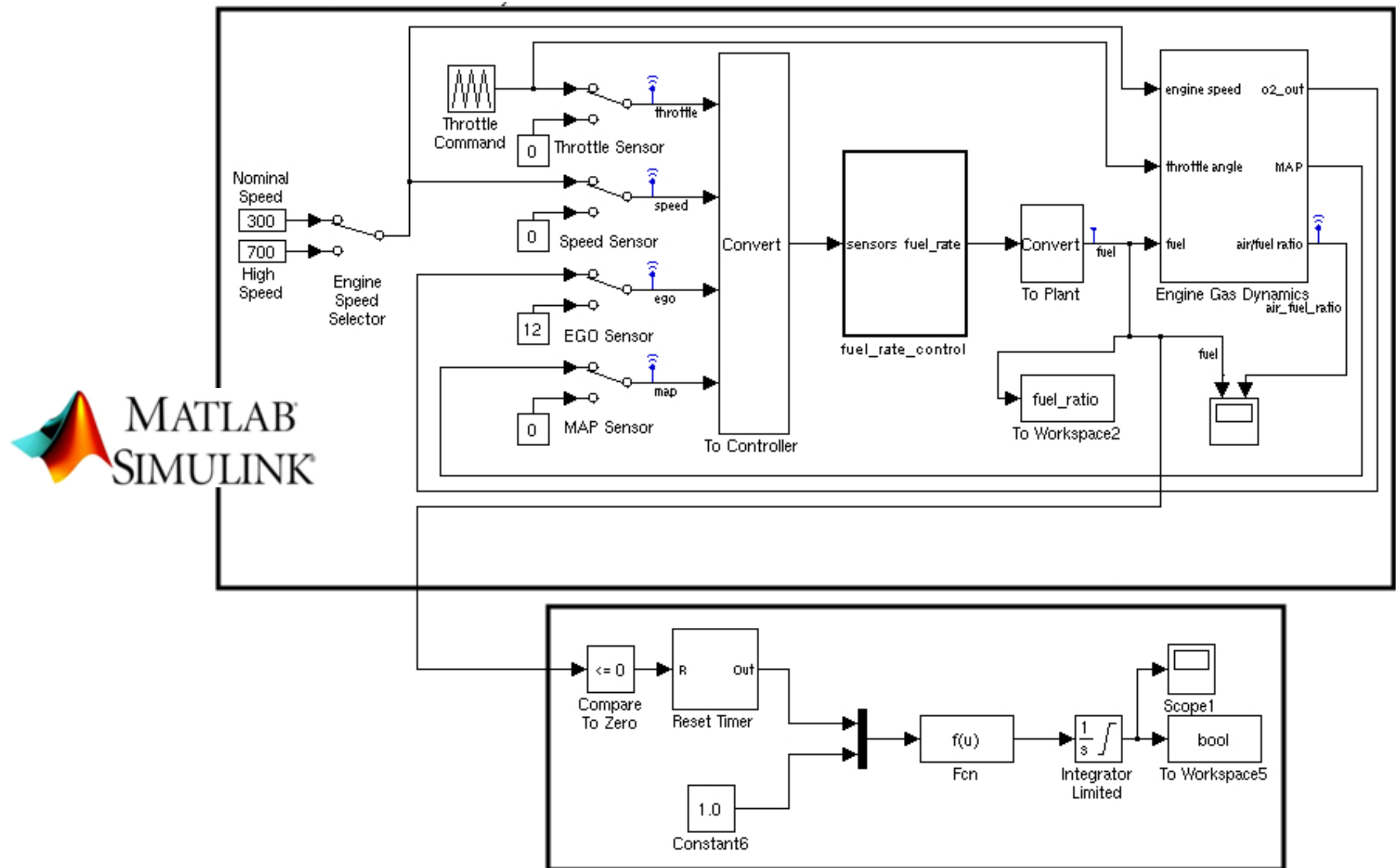


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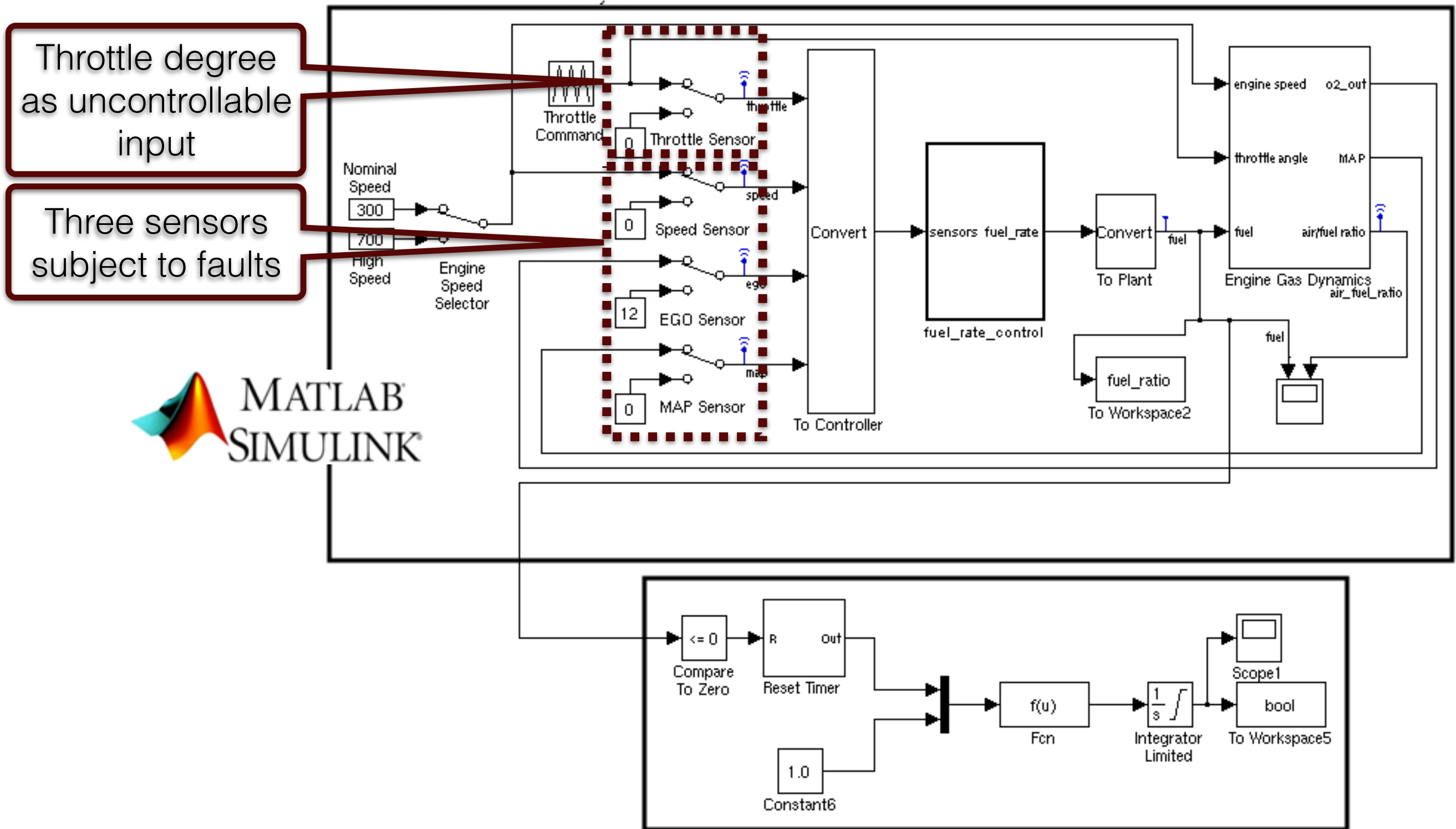
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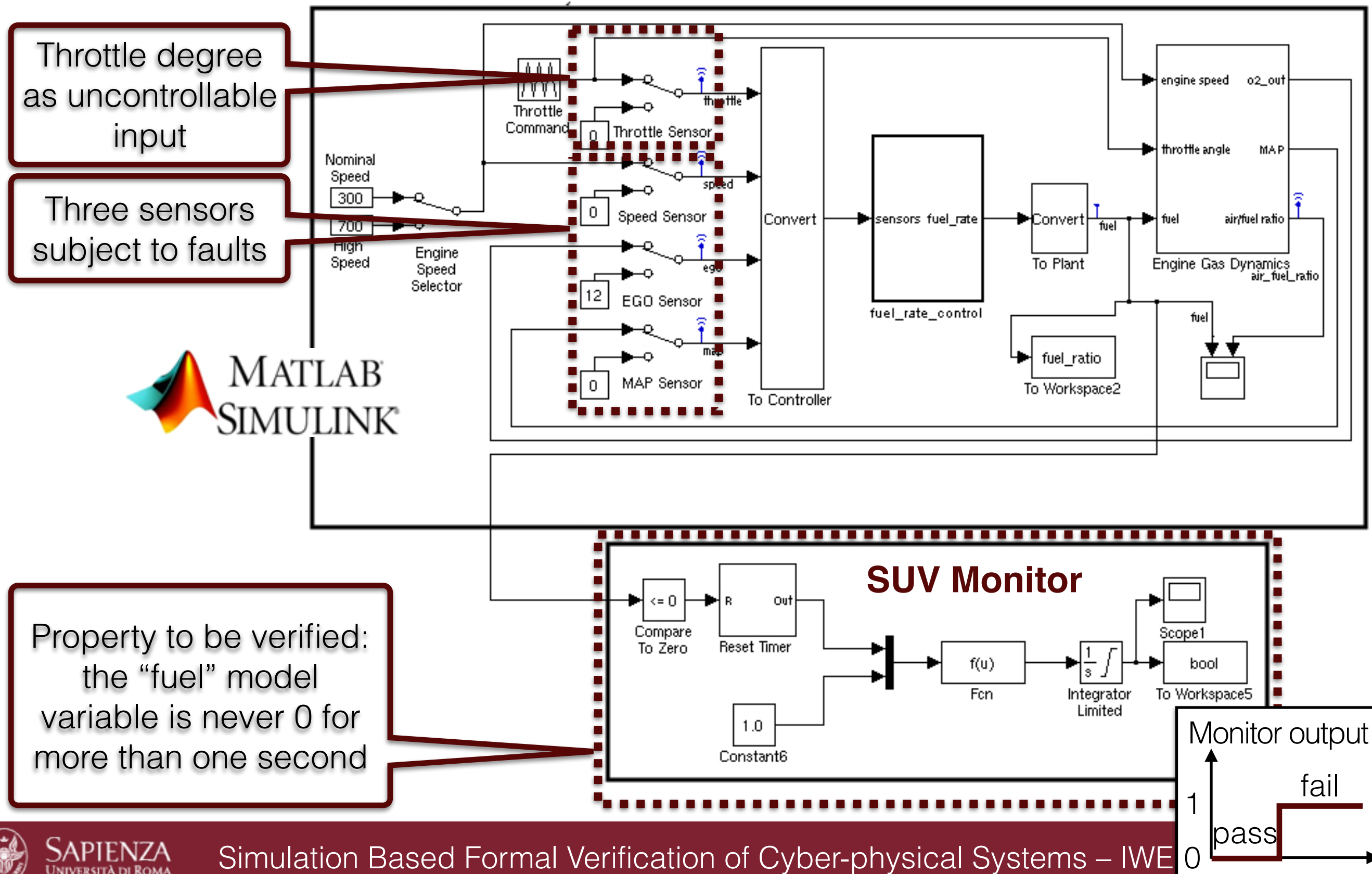
Experiments: Fuel Control System



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Experiments: Disturbance Models

Two disturbance models:

- sensor faults repaired after 1 second
- at most one fault active at any time
- **Model $\mathcal{D}_1$** : $h = 100$ sec, $\tau = 1$ s $\longrightarrow$ **4M dist. traces**
- **Model $\mathcal{D}_2$** : $h = 200$ sec, $\tau = 500$ ms $\longrightarrow$ **13M dist. traces**

Disturbance model CMurphi encoding

```
Ruleset d : FAULT_TYPE do
  Rule "Inject Fault"
    time_since_last_fault[d] = -1 &
    no_fault_needs_repair() &
    num_faults < MAX_NUMFAULTS &
    num_active_faults() < MAX_NUMACTIVEFAULTS
  ==> begin
    time_since_last_fault[d] := 0;
    num_faults := num_faults+1;
    time_step();
  end;

  Rule "Repair Fault"
    time_since_last_fault[d] = FAULT_DURATION
  ==> begin — repair fault d
    time_since_last_fault[d] := -1;
    time_step();
  end;
End;
```

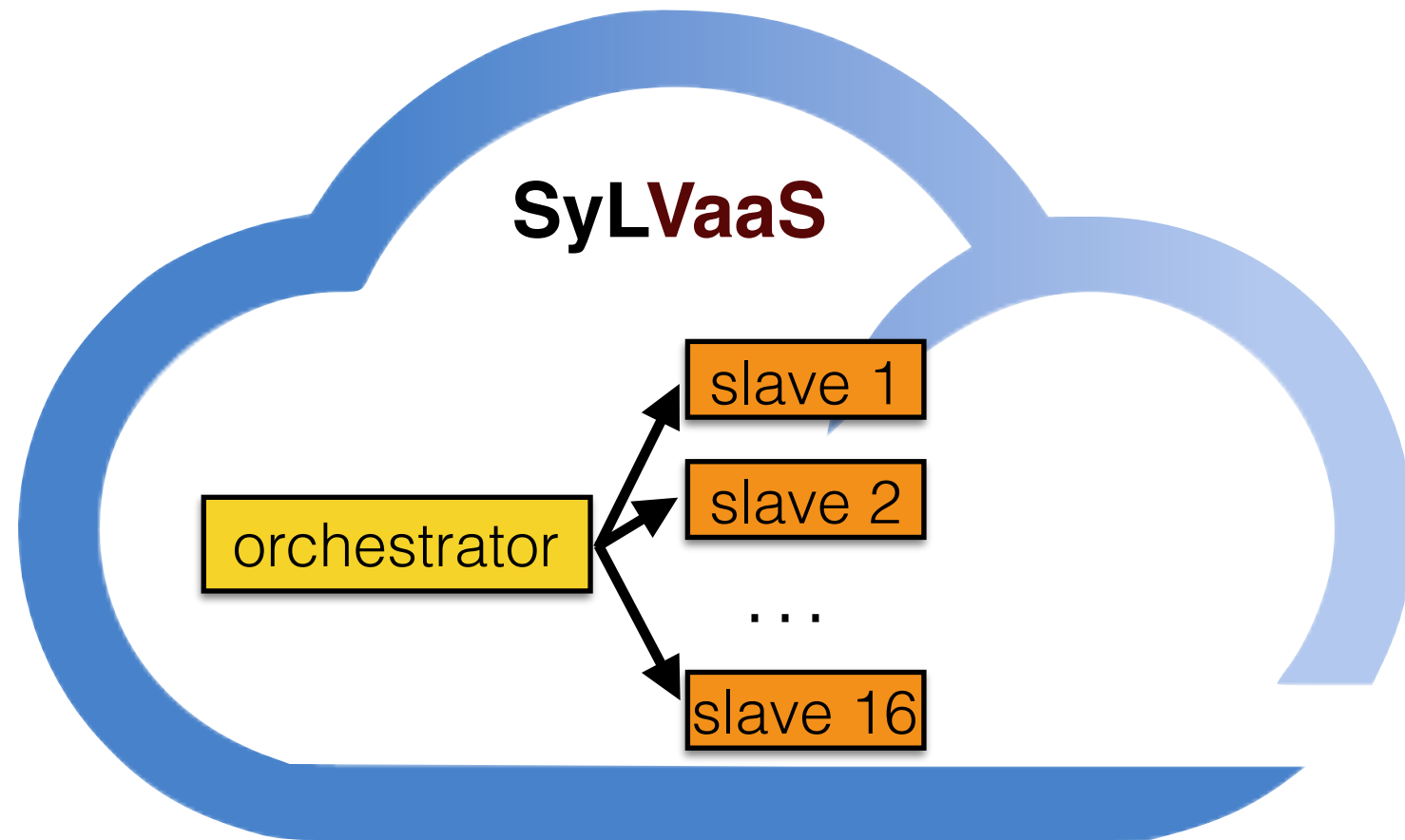
```
Ruleset d : INPUT_TYPE do
  Rule "Inject Input Variation"
    no_fault_needs_repair() &
    num_inputs < MAX_NUMINPUTS &
    is_input_variation_allowed()
  ==> begin
    num_inputs := num_inputs + 1;
    time_step();
  end;
End;

Rule "No Disturbance"
  no_fault_needs_repair() ==>
  begin time_step(); end;
...
Finalstate "Correct Length"
  no_faults() & num_faults <= MAX_NUMFAULTS &
  num_inputs <= MAX_NUMINPUTS;
```

Experiments: Infrastructure

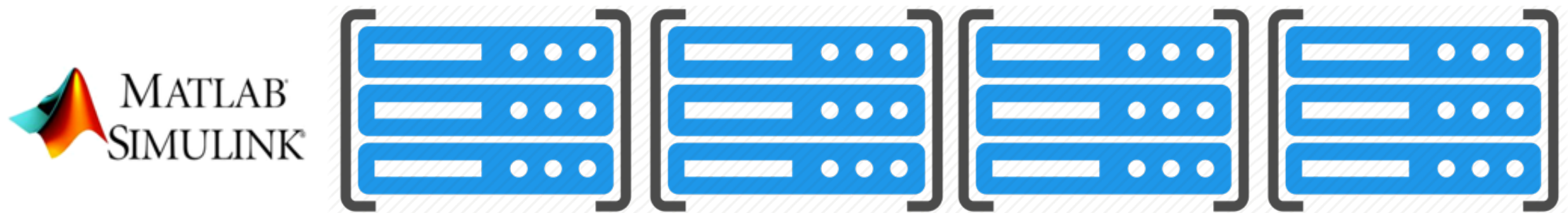
SyLVaaS infrastructure:

- 1 orchestrator
- 1 to 16 slaves



User private cluster:

- 8 to 64 8-core machines
—> **up to 512 Simulink parallel instances**



Experiments: Trace Generation & Slicing

Parallel generation of disturbance traces

4M traces

13M traces

#slaves (S)	disturbance model $\mathcal{D}_1$			disturbance model $\mathcal{D}_2$		
	time (h:m:s)	speedup	efficiency	time (h:m:s)	speedup	efficiency
1	0:32:32	$1.00\times$	100.00%	4:45:47	$1.00\times$	100.00%
8	0:5:32	$5.88\times$	73.50%	0:43:2	$6.64\times$	83.00%
16	0:3:11	$10.22\times$	63.88%	0:26:16	$10.88\times$	68.00%

Slicing of disturbance traces

#slices (k)	$\mathcal{D}_1$ (h:m:s)	$\mathcal{D}_2$ (h:m:s)
128	0:4:1	0:8:7
256	0:4:32	0:11:25
512	0:4:52	0:13:17

Experiments: Random Exhaustive Campaigns

Computation of random exhaustive optimised simulation campaigns:

4M traces

13M traces

	disturbance model $\mathcal{D}_1$		disturbance model $\mathcal{D}_2$	
#slices (k)	sim. campaign comp. time (h:m:s)	overall time (h:m:s)	sim. campaign comp. time (h:m:s)	overall time (h:m:s)
128	0:1:44	0:8:56	0:4:1	0:38:24
256	0:0:42	0:8:25	0:2:27	0:40:8
512	0:0:13	0:8:16	0:0:24	0:39:57

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Computation of **optimised random exhaustive** simulation campaigns via **embarrassing parallelism** (16 cores)

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Overall SyLVaaS **response time**
(gen+slicing+sim.camp.comp.)

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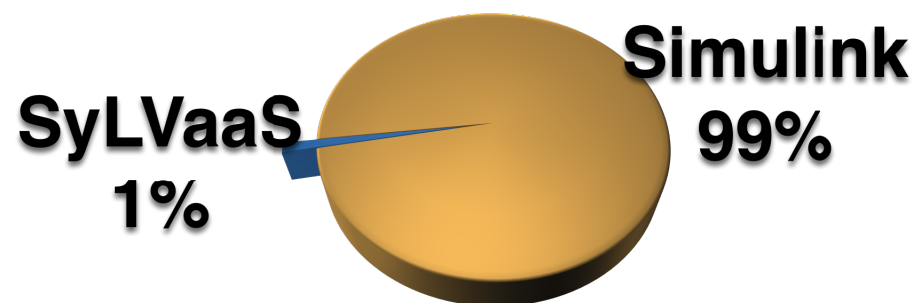
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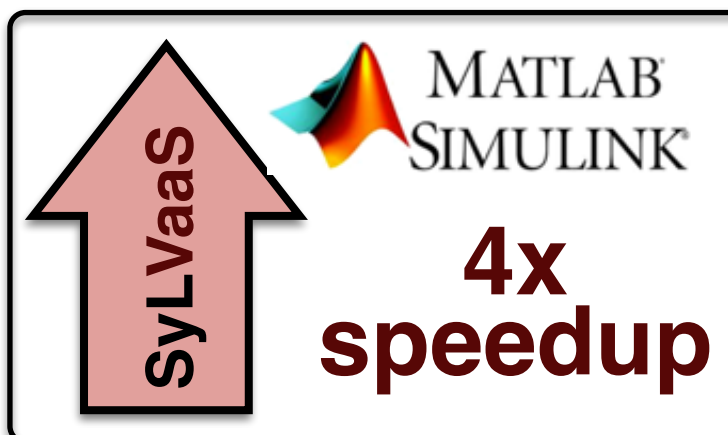
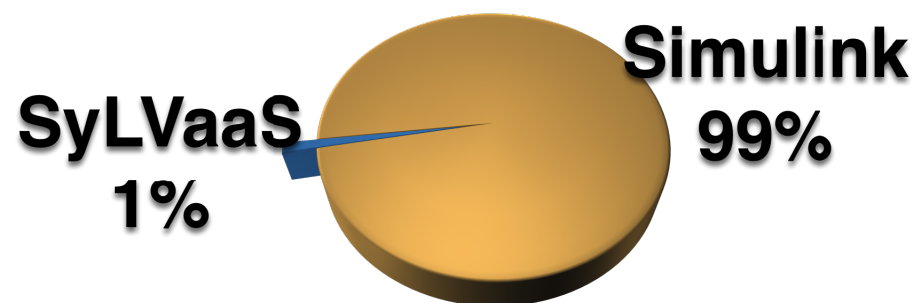
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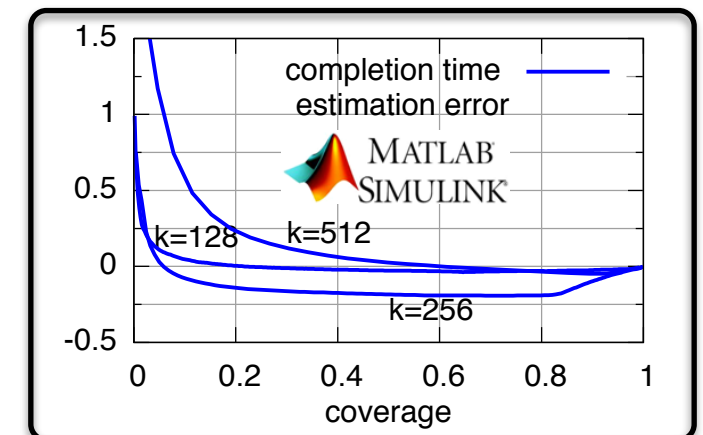
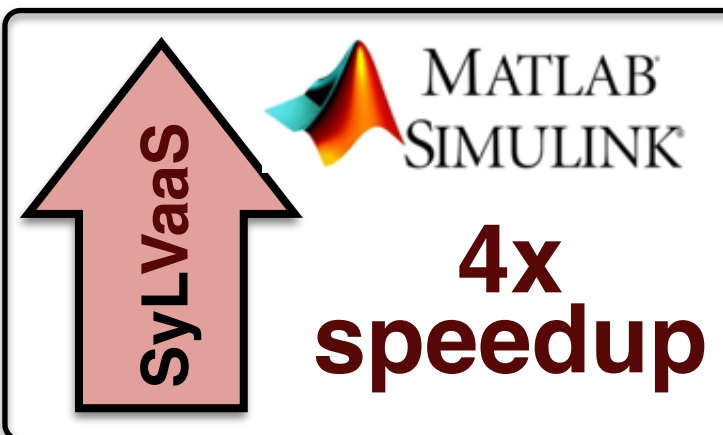
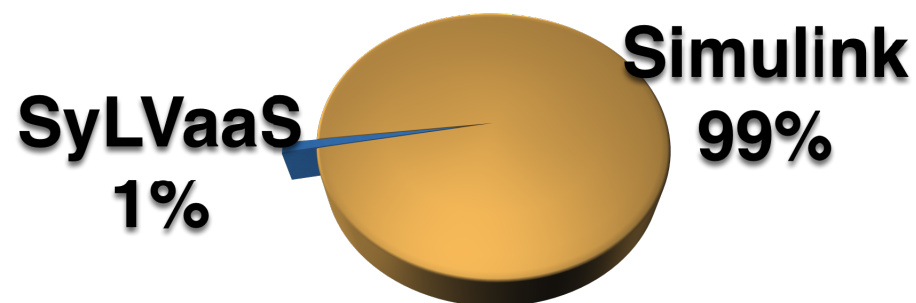
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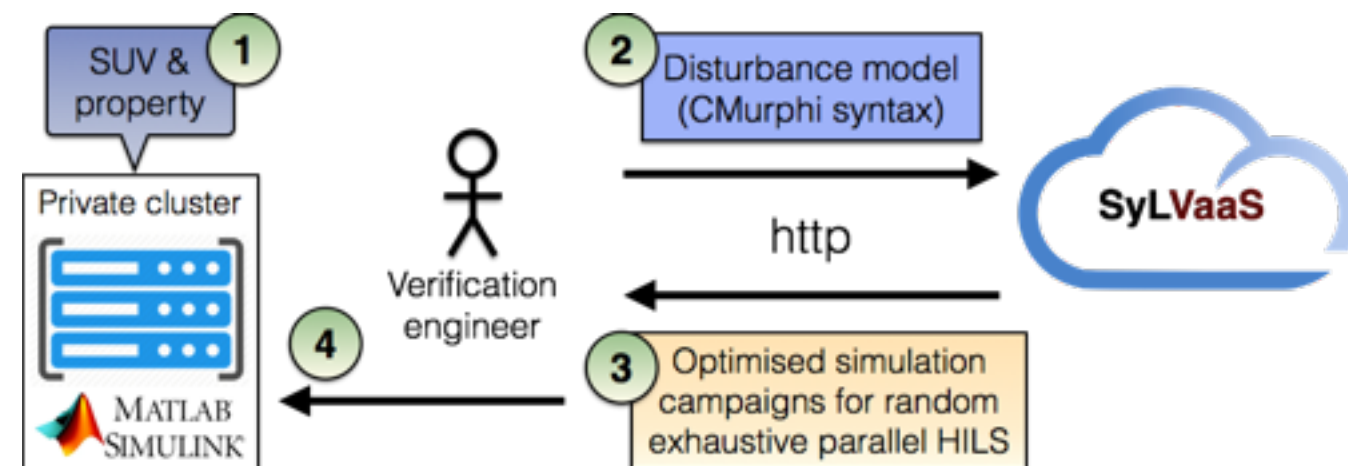
SyLVaaS vs. **Simulink**



Conclusions

SyLVaaS: System Level Verification as a Service

- Given formal model of **operational environment**
- Efficiently computes **random exhaustive simulation campaigns**
- **Approach scales well**: additional experiments with dist. models yielding **40M traces**
- Campaigns run **embarrassingly in parallel** on all Simulink instances available on private user cluster
- Campaigns **optimise** simulation activities (**4x speedups**) by storing/restoring intermediate simulation states as much as possible (depending on available mass memory space on user cluster)
- **Graceful degradation**: omission probability bound available anytime during verification
- **Completion time estimation** available anytime during verification
- Both SUV model and property to be verified kept secret (**Intellectual Property protection**)





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Thank you!

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