HEPSYCODE

A System-Level Methodology for HW/SW Co-Design of Heterogeneous Parallel Dedicated Systems

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Overview

- The Proposed Methodology
  - System Behaviour Specification
  - Functional Simulation
  - Co-Analysis & Co-Estimation
    - Technologies Library
    - Co-Analysis
    - Co-Estimation
  - Design Space Exploration
    - HW/SW Partitioning, Mapping and Architecture Definition
    - Timing Co-Simulation
    - Iterations
    - Example
- Main References

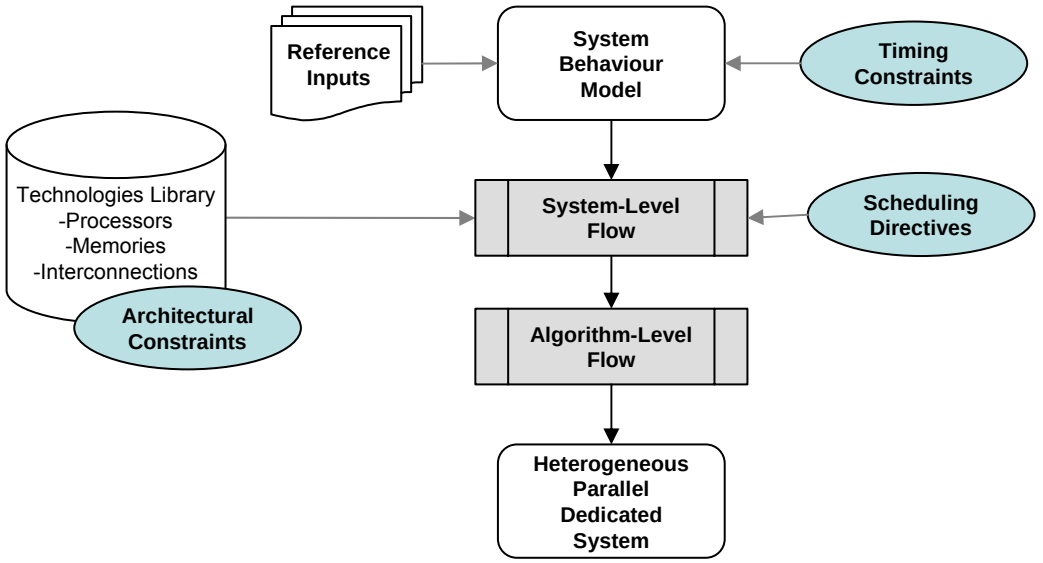
The Proposed Methodology

The Proposed Methodology

- The proposed methodology starts from a model of the system behaviour, based on a *Concurrent Processes MoC*, and lead to an heterogeneous parallel dedicated system able to satisfy given F/NF requirements
  - In particular, the goal is to suggest to designer
    - **How to partition processes between HW and SW**
    - **Which kind of heterogeneous parallel architecture to use**
      - How many processors, which kind, how to connect them
    - **How to map processes to processor**
      - GPP, ASP, SPP
  - *Current NF requirements are mainly architectural and timing constraints but the methodology can be extended*
    - *e.g. power/energy, reliability, monitorability, mixed-criticality*

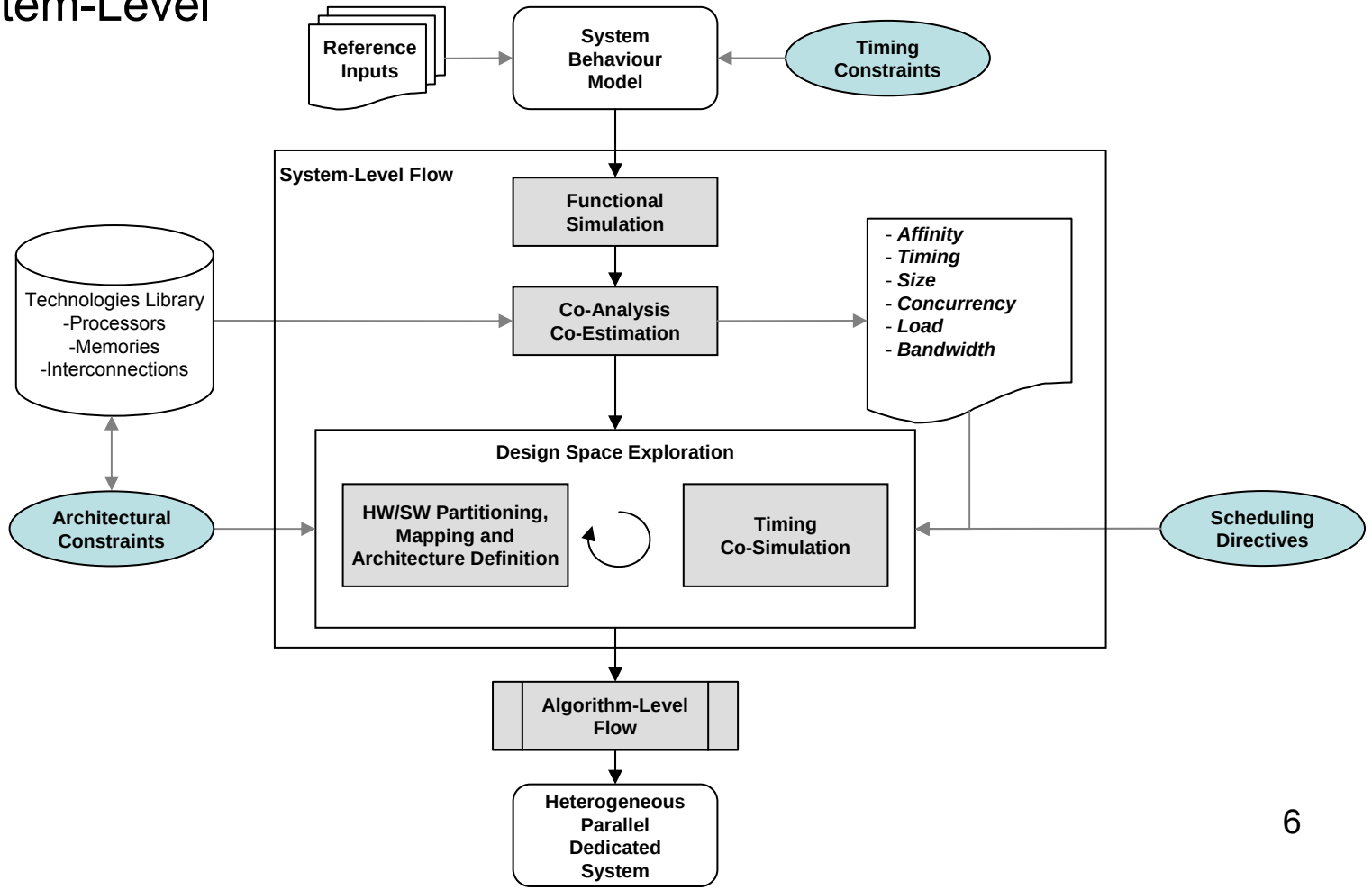
The Proposed Methodology

- **Reference Co-Design Flow**



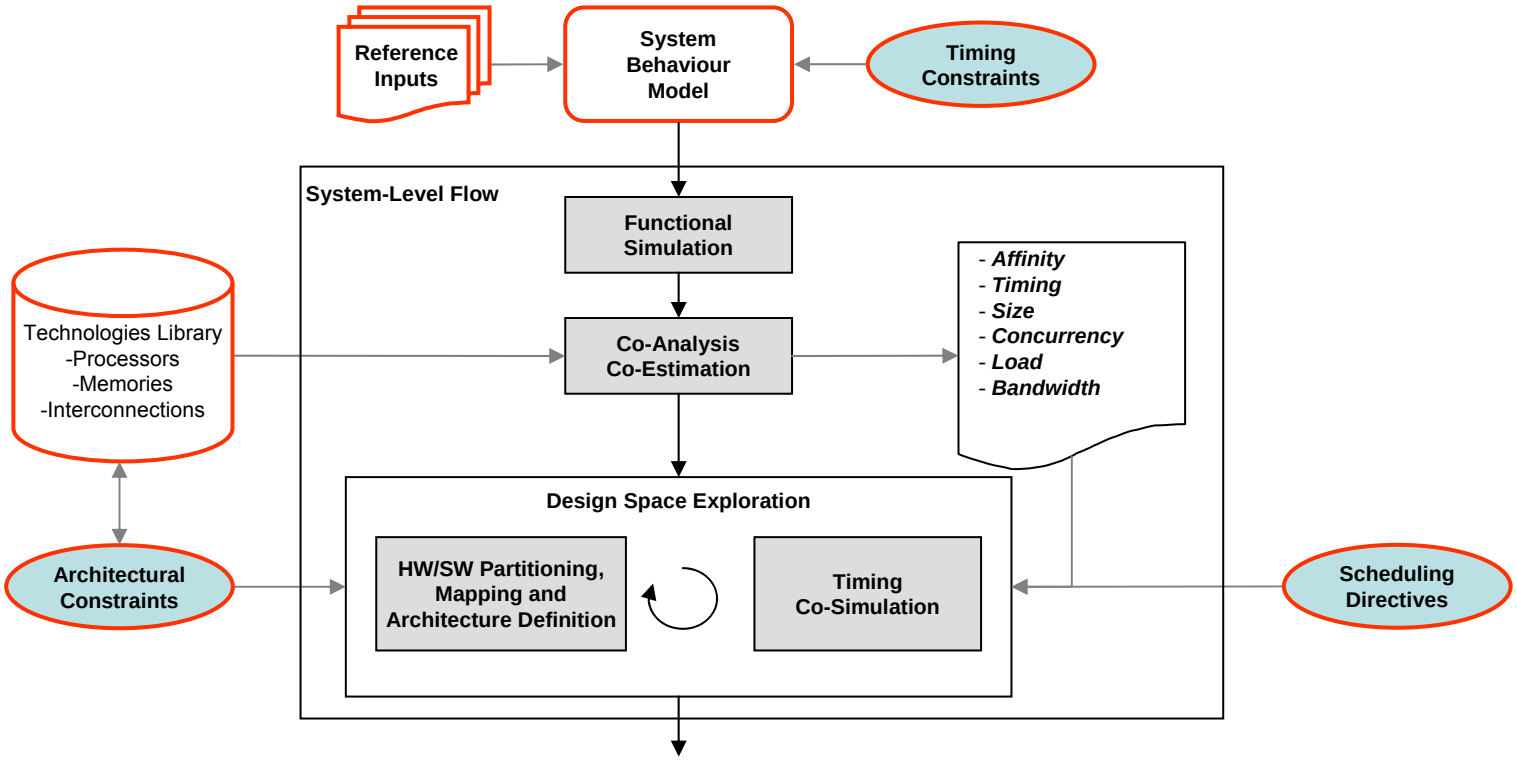
The Proposed Methodology

- **Reference Co-Design Flow**
  - System-Level



The Proposed Methodology

- **Inputs**



The Proposed Methodology

- **Inputs**
  - Functional Requirements
    - ***System Behaviour Model***
      - An executable/simulatable model of the system behaviour based on a *Concurrent Processes MoC*
    - ***Reference Inputs***
      - Relevant inputs data sets

The Proposed Methodology

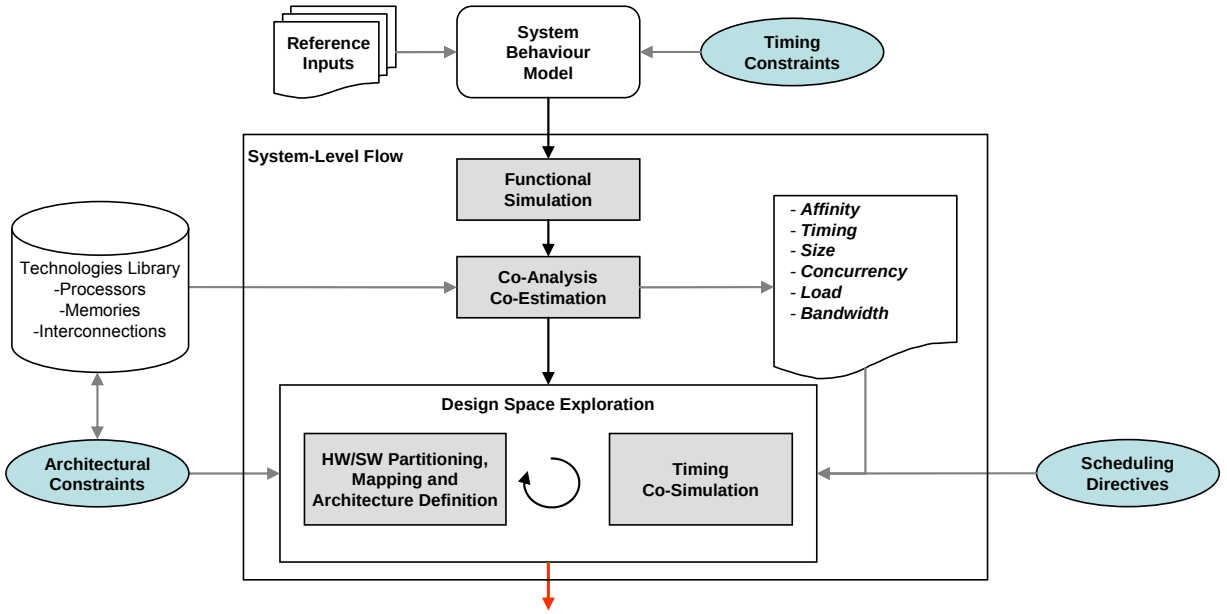
- **Inputs**
  - Non–Functional Requirements/Constraints
    - *Timing Constraints*
      - ***Time-To-Completion constraint***
        - » Actually the only timing one (WIP: real-time constraints)
    - *Architectural Constraints*
      - ***Target Form Factor (TFF)***
        - » *ASIC, FPGA, SOB (PCB), SO(P)C*
      - ***Target Template Architecture (TTA)***
        - » min/max # of *processors* and *interconnection links* instances
        - » Total available area (or an equivalent metric)
    - ***Scheduling Directives***
      - Available scheduling policies
        - » RR, Priority, HPV, etc…

The Proposed Methodology

- **Inputs**
  - ***Technologies Library***
    - Characterization of the available processors, memories and links
      - Actual attributes are dependent on TFF
        - » ASIC, FPGA, SOB, SO(P)C

The Proposed Methodology

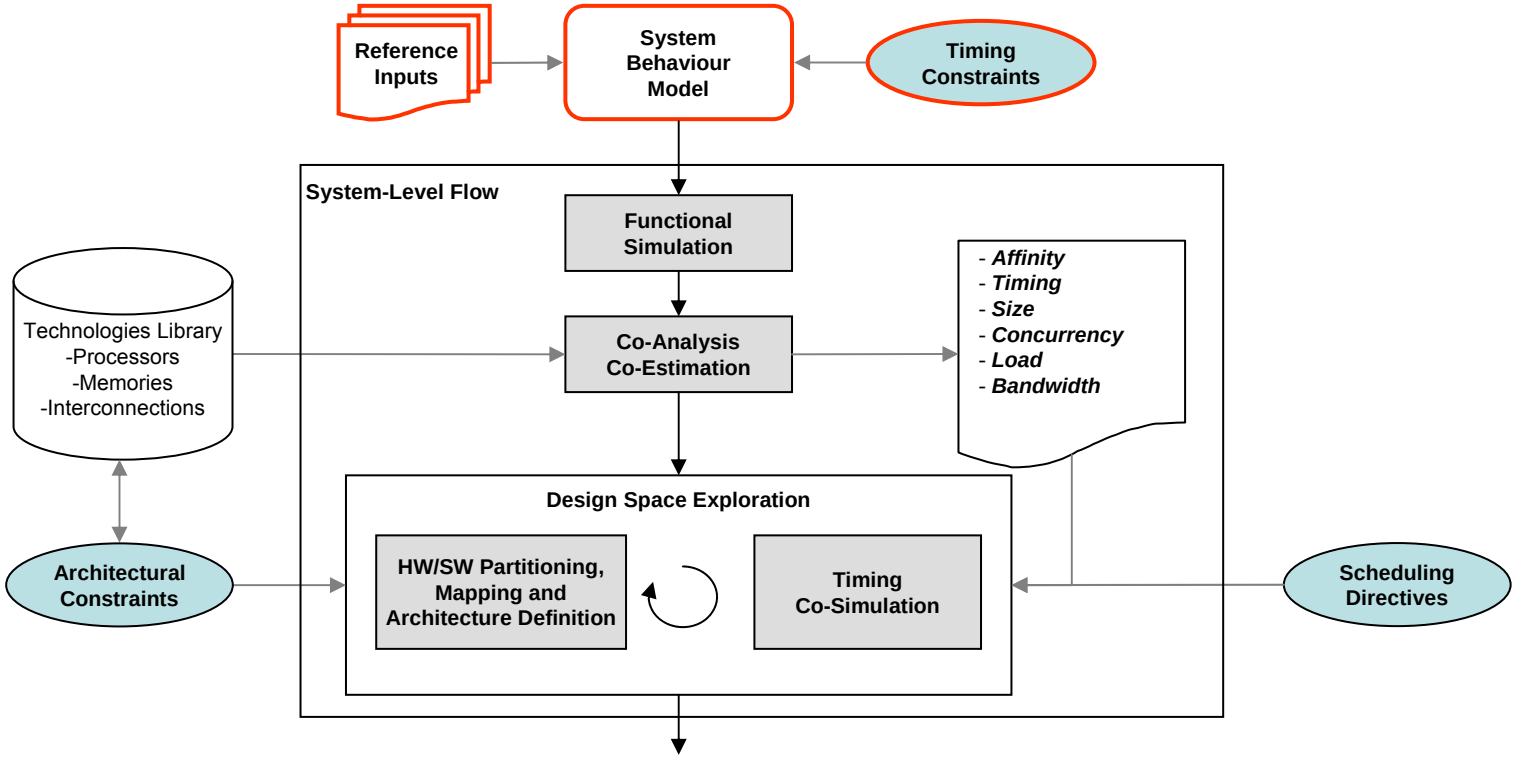
- **Outputs**
  - Definition of an heterogeneous parallel dedicated system
    - **HW/SW partitioning of processes**
    - **HW/SW Architecture**
      - How many processors, which kind, how to connect them, which scheduling policies on SW processors
    - **How to map processes to processors**



The Proposed Methodology

System Behaviour Specification

System Behaviour Specification



System Behaviour Specification

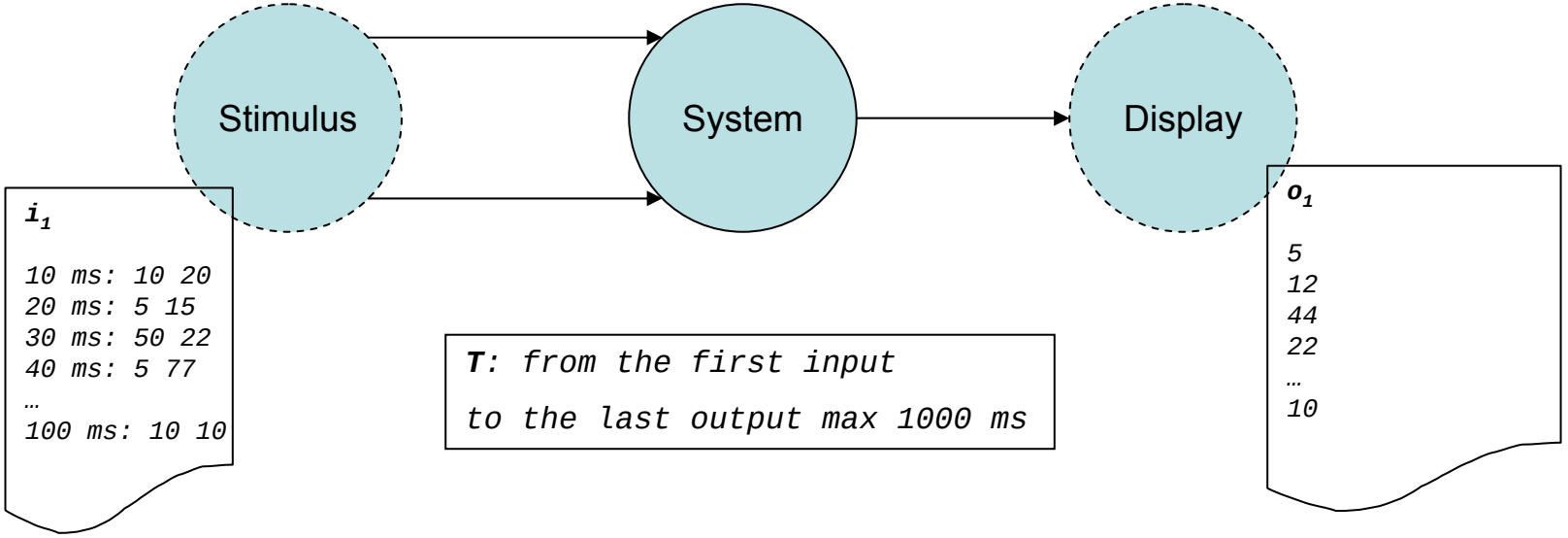
- ***SBS = {SBM, RI, T}***
  - **SBM** = {PS, CH}: Concurrent Processes MoC → **CSP-based**
    - A MoC that explicitly defines also a model of communication
      - Unidirectional point-to-point blocking channels for data exchange
    - Such a MoC is well suited to describe system-level behaviour since it is unifying for HW and SW and it enables the “processes to processors” mapping
      - Languages suitable to describe CSP
        - » **SystemC**, OCCAM, Handel-C, ADA
      - More abstract languages
        - » UML, SysML, Simulink

System Behaviour Specification

- ***SBS = {SBM, RI, T}***
  - ***RI:*** a set of inputs (possibly timed), representative AMAP of typical operating conditions of the system and related expected outputs
    - To be used for analysis and validation
  - ***T***: time-to-completion timing constraint
    - To be satisfied by each RI

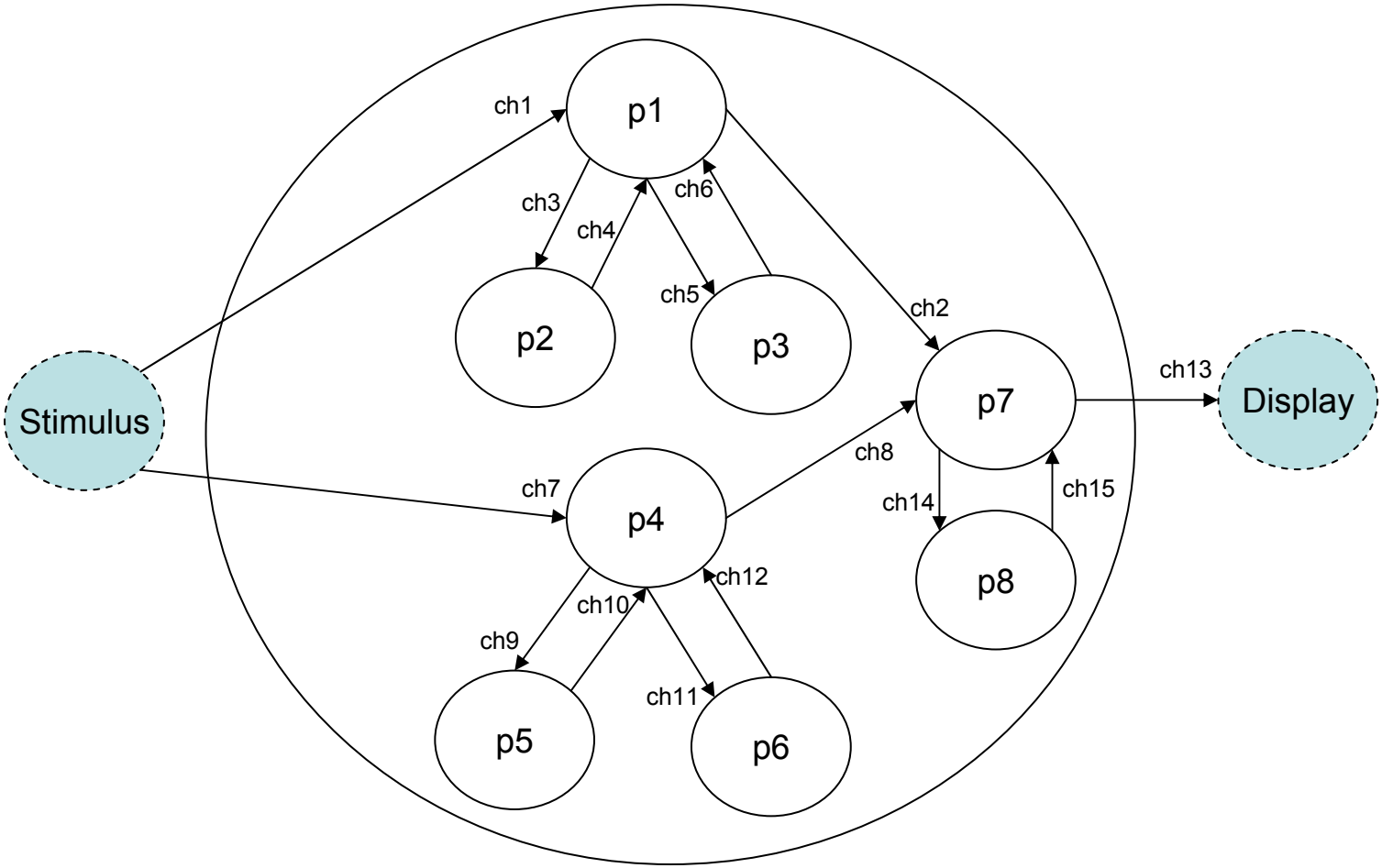
System Behaviour Specification

- Reference Example
  - *RI*
  - *T: 1000 ms*



System Behaviour Specification

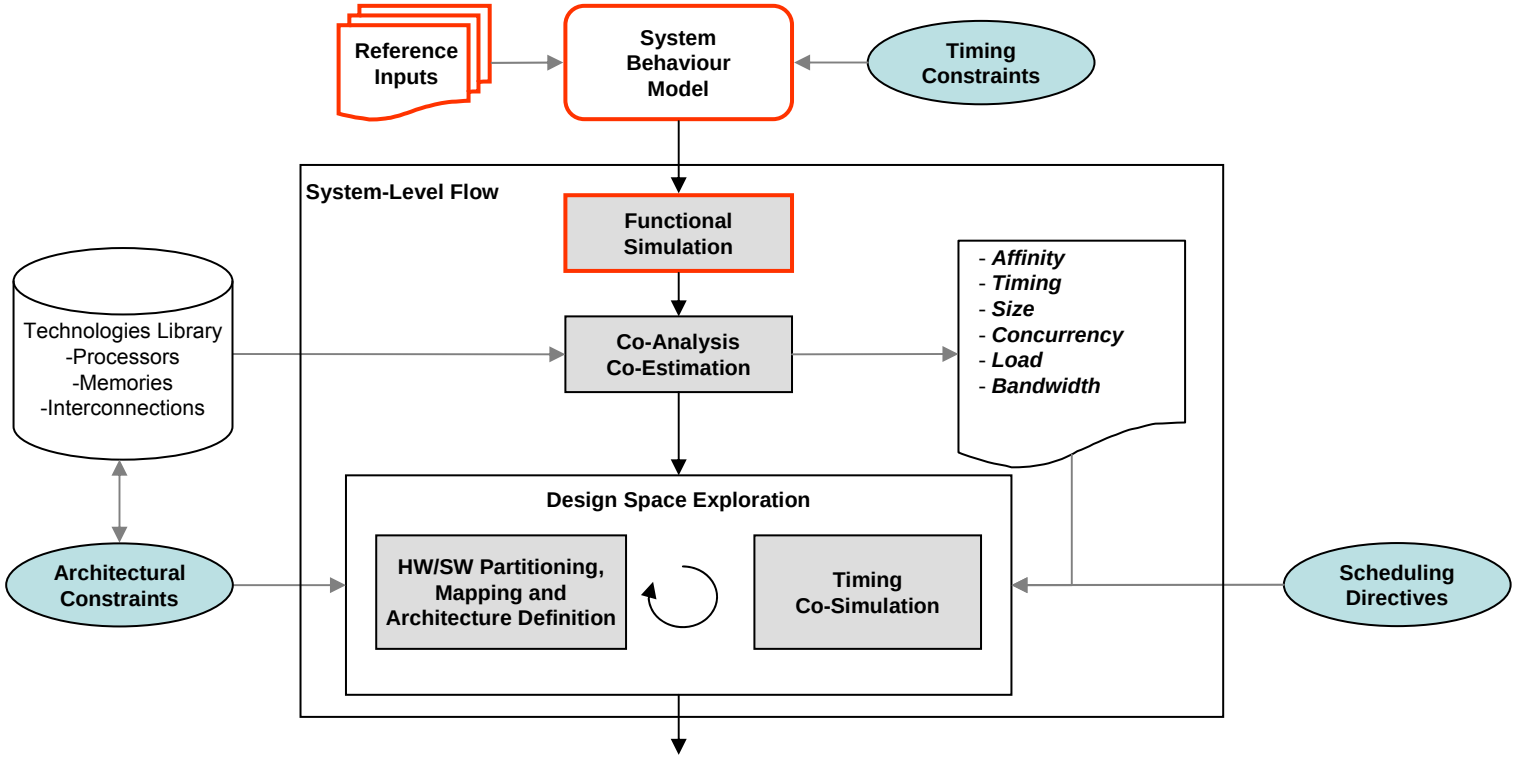
- Reference Example
  - *PS and CH*



The Proposed Methodology

Functional Simulation

Functional Simulation



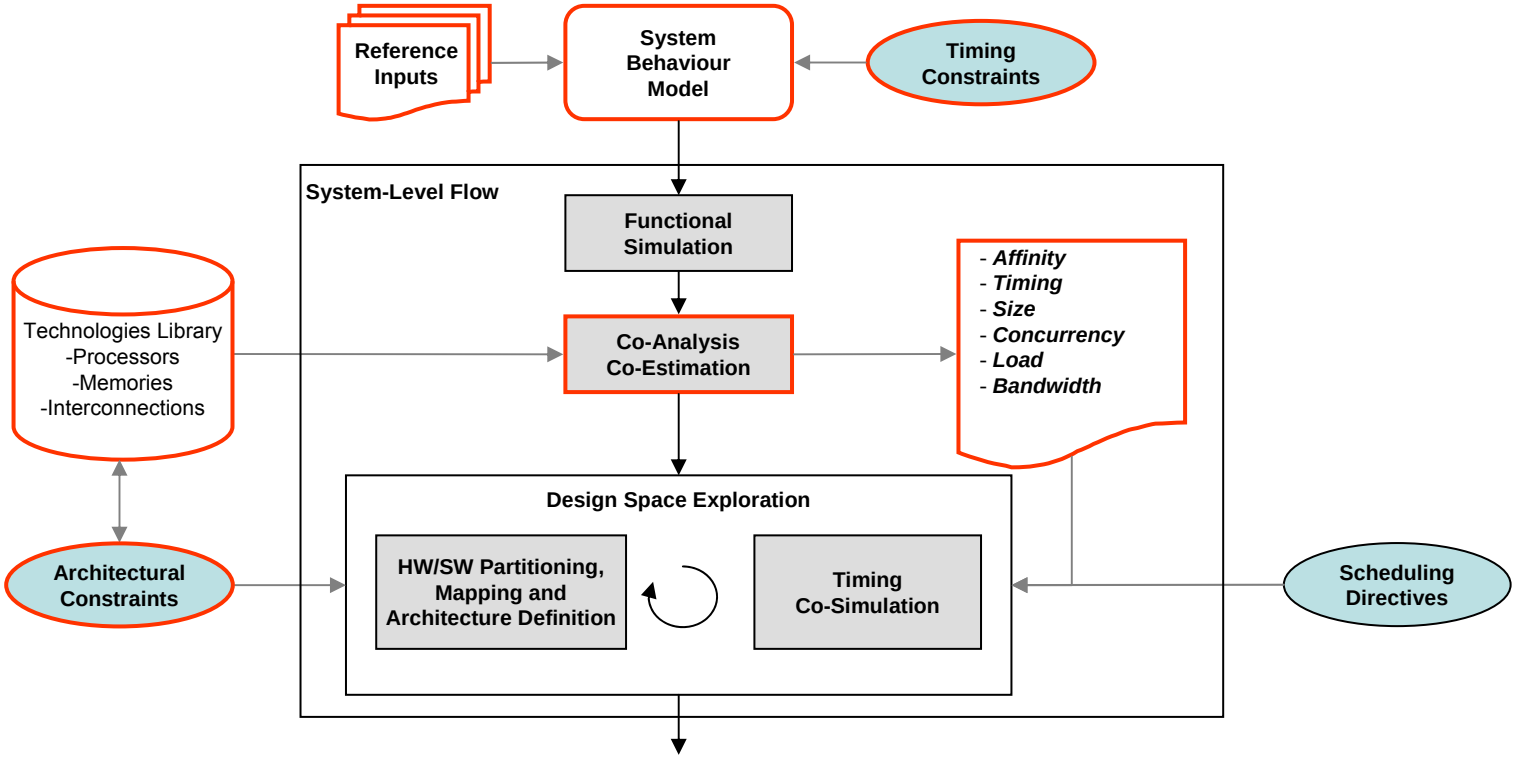
Functional Simulation

- This step allows to “validate” the SBM by means of a functional simulation
  - Such a simulation allows to take into account timed inputs (i.e. there is a concept of simulated time), but it doesn’t consider the time that will be needed to execute the statements composing the processes and for the communications
    - Currently based on standard SystemC kernel
  - If SBM is not correct (i.e. wrong outputs or critical conditions such as e.g. deadlocks) SBM should be properly modified and simulated again

The Proposed Methodology

Co-Analysis & Co-Estimation

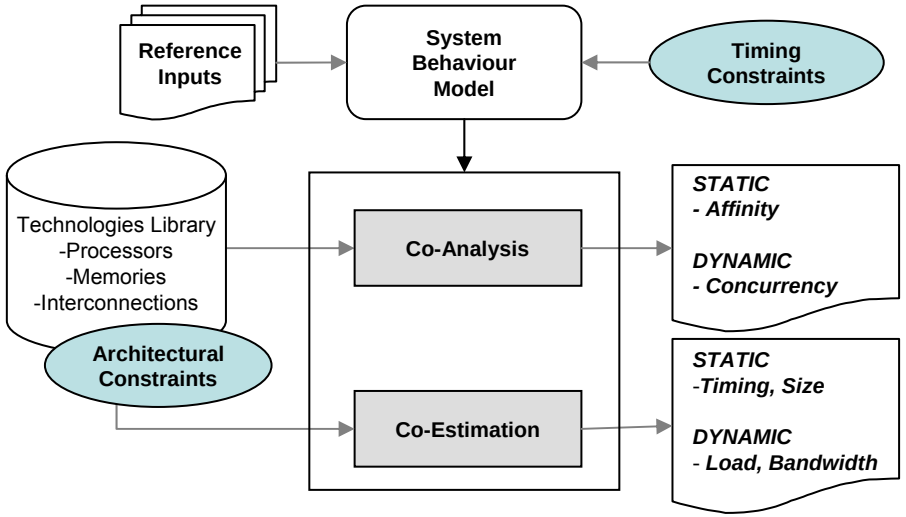
Co-Analysis & Co-Estimation



Co-Analysis & Co-Estimation

- This step is composed of two independent activities
  - Co-Analysis
    - *Static* and *Dynamic*
  - Co-Estimation
    - *Static* and *Dynamic*

- Both are based on a given ***Technologies Library***



The Proposed Methodology

Co-Analysis & Co-Estimation

Technologies Library

Technologies Library

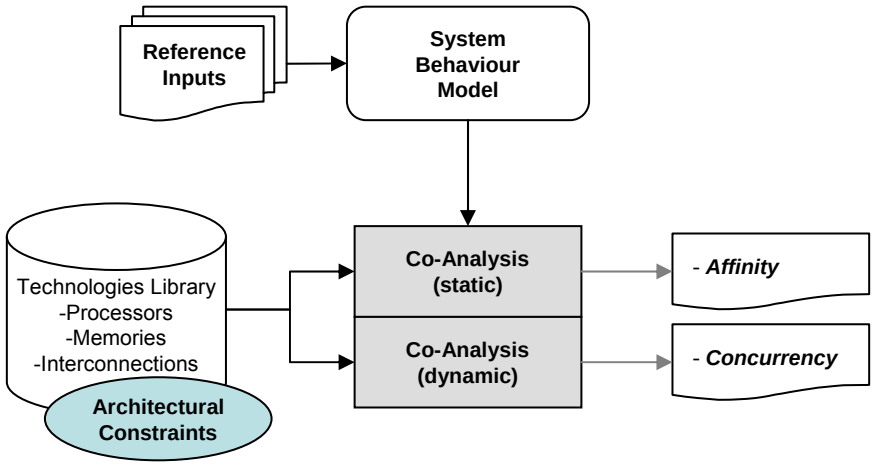
- TL contains the characterization of available processors, interconnection links and memories
  - It is used to perform analysis and estimations and, later, to build the final architecture during the DSE step
    - However, there is the need for different TLs depending on TFF
      - The main differences are related to the different attributes (or different meaning of the same attribute)
  - In general
    - ***TL*** *= {PC, IL, M}*
      - ***PC****: {pc_1, …, pc_n}*
        - » *Set of processors*
      - ***IL****: {il_1, …, il_n}*
        - » *Set of interconnection links*
      - ***M***: *{m_1,…m_n}*
        - » *Set of memories*

The Proposed Methodology

Co-Analysis & Co-Estimation

Co-Analysis & Co-Estimation

- Co-Analysis
  - This activity performs the evaluation of two kinds of metrics
    - *Static analysis*
      - ***Affinity***
    - *Dynamic analysis*
      - ***Concurrency***

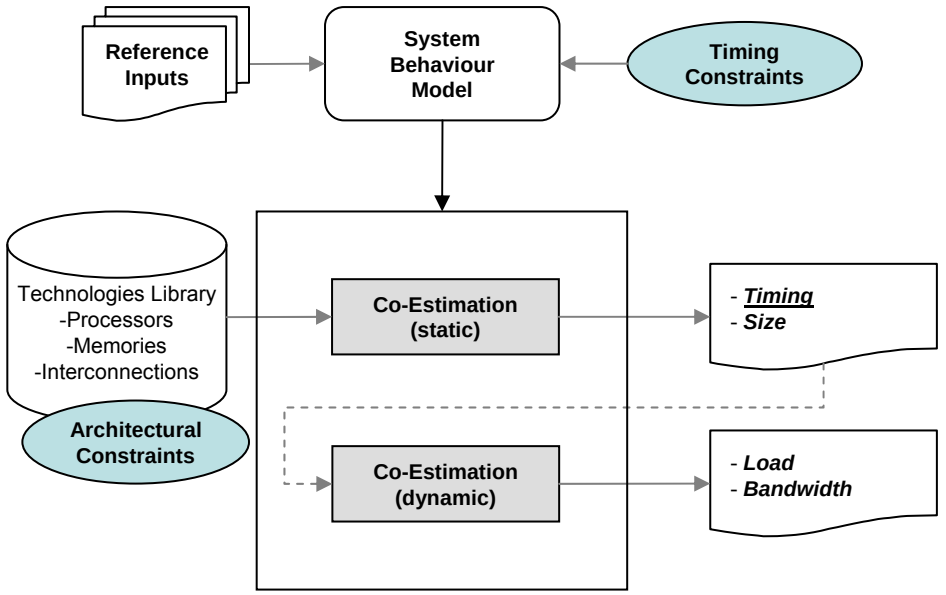


The Proposed Methodology

Co-Analysis & **Co-Estimation**

Co-Analysis & Co-Estimation

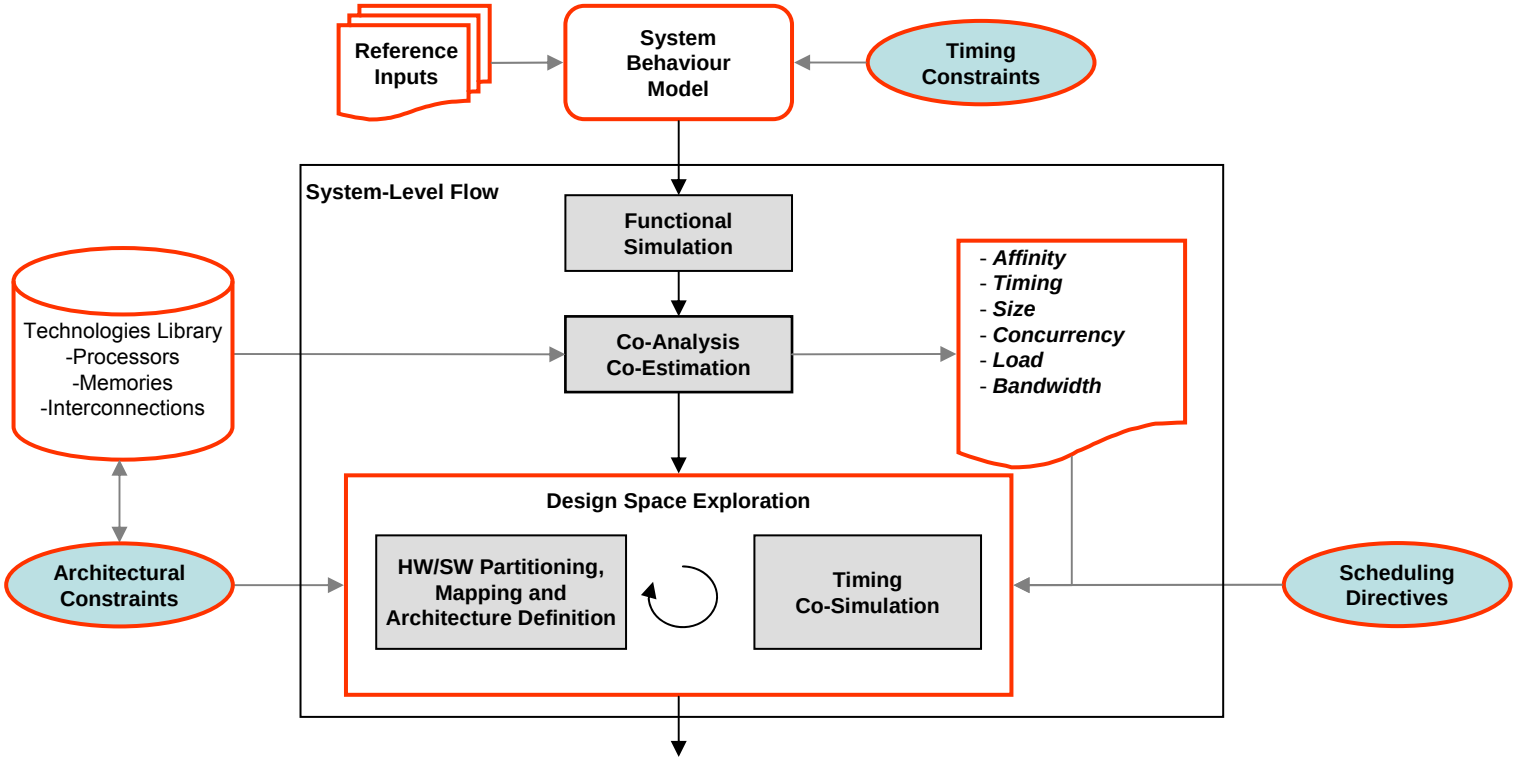
- Co-Estimation
  - This activity performs two kinds of dependent estimations
    - *Static estimations*
      - ***Timing***
      - ***Size***
    - *Dynamic estimations*
      - ***Load***
      - ***Bandwidth***



The Proposed Methodology

Design Space Exploration

Design Space Exploration



Design Space Exploration

- This step is composed of two iterative activities
  - HW/SW Partitioning, Mapping and Architecture Definition
  - Timing Co-Simulation

  - The final goal is the automatic identification of
    - an HW/SW partitioning of the processes in PS
    - an heterogeneous parallel architecture composed of several connected *processors with local memory* (i.e. *blocks*) composed starting form the TL and able to satisfy the architectural constraints
    - a mapping of the partitioned processes to the *blocks* able to satisfy the timing constraint

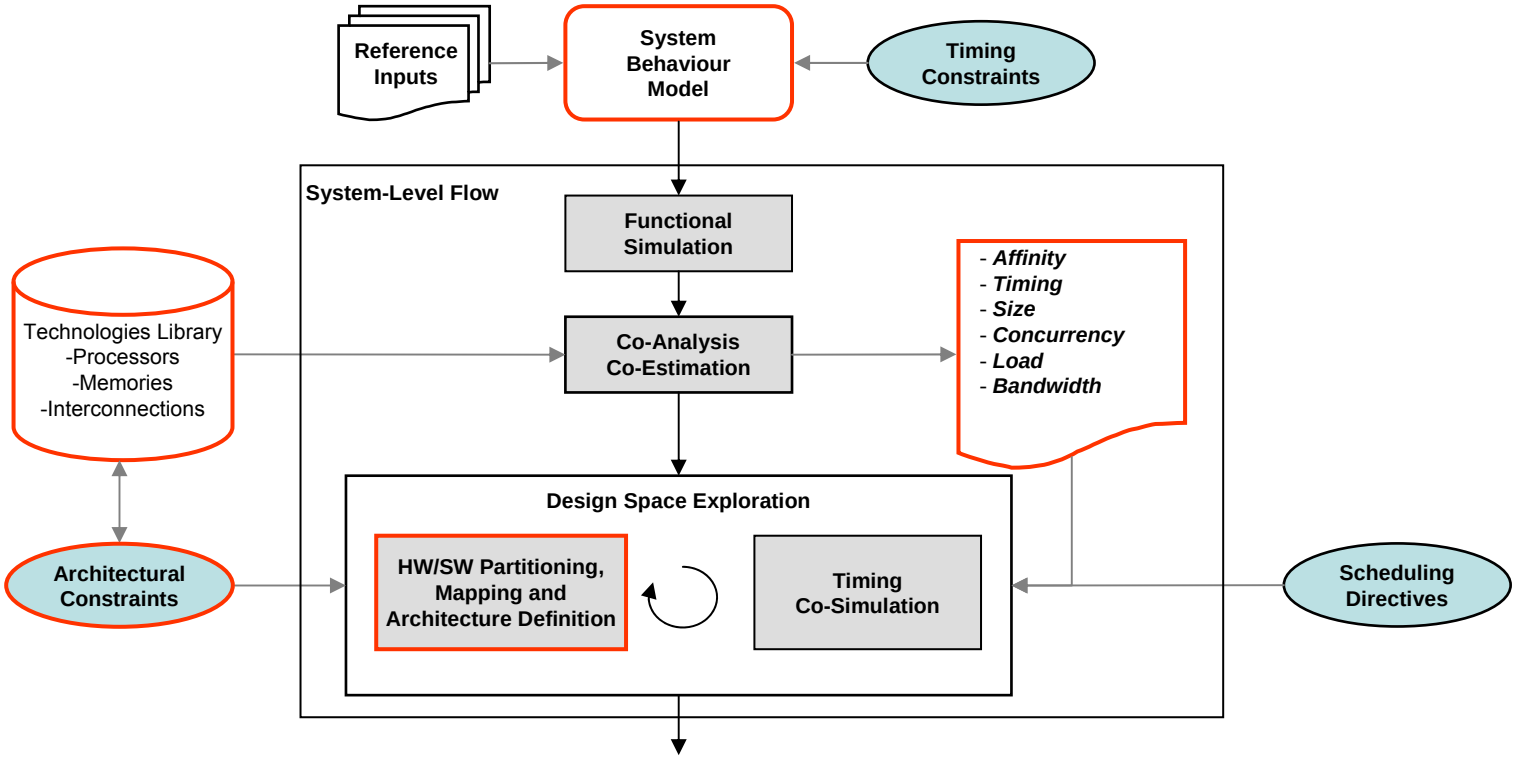
The Proposed Methodology

Design Space Exploration

HW/SW Partitioning, Mapping and Architecture Definition

Design Space Exploration

HW/SW Partitioning, Mapping and Architecture Definition

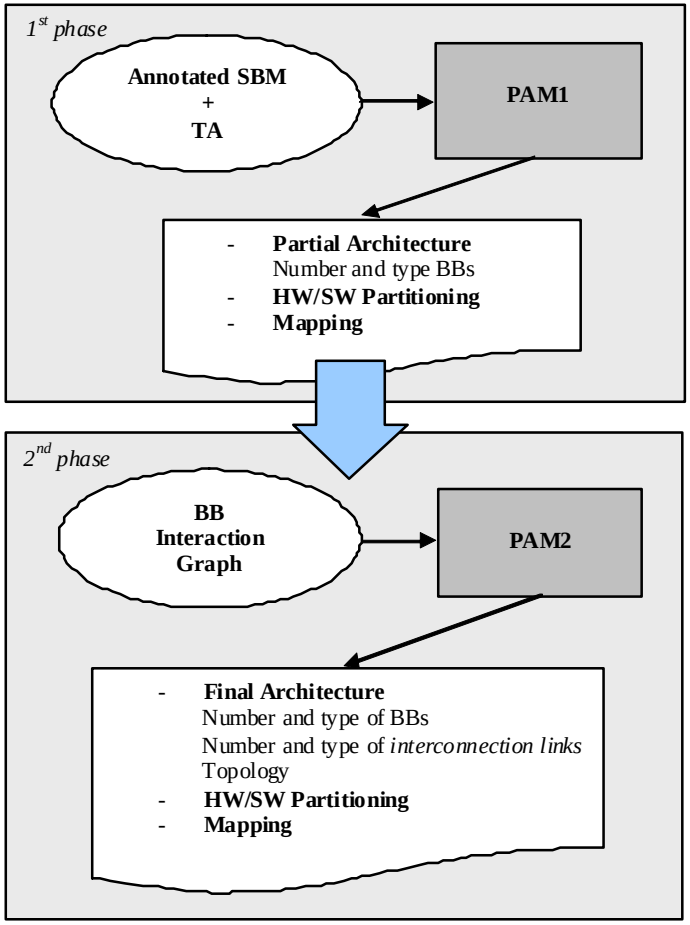


Design Space Exploration

- HW/SW Partitioning, Mapping and Architecture Definition
  - Main inputs
    - *Annotated SBM*
      - *SBM + Process-level metrics/estimations*
    - *Technology Library*
    - *Architectural Constraints*
      - To limit cost, to ensure feasibility, or to model an existing platform

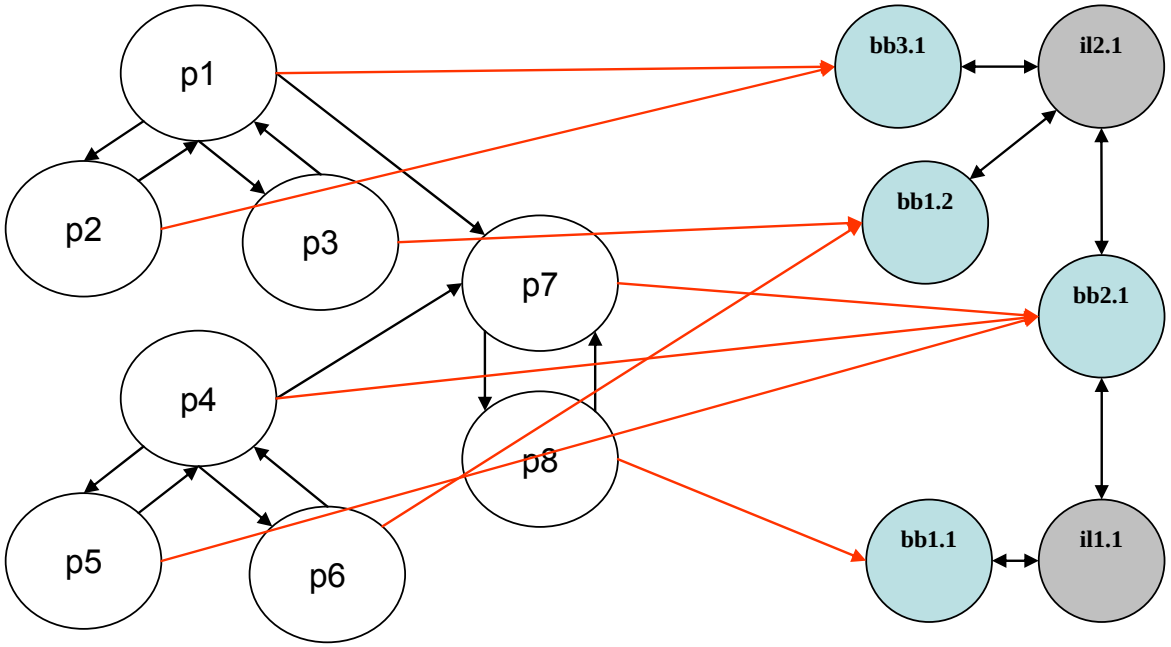
Design Space Exploration

- HW/SW Partitioning, Mapping and Architecture Definition
  - 2 Phases Approach



Design Space Exploration

- HW/SW Partitioning, Mapping and Architecture Definition
  - Main Outputs
    - *Heterogeneous Parallel Dedicated Systems (HPDS)*
      - A set of blocks connected by means of a set of links
        - » *Architecture Graph*
    - *Mapping between SBM and blocks/links*



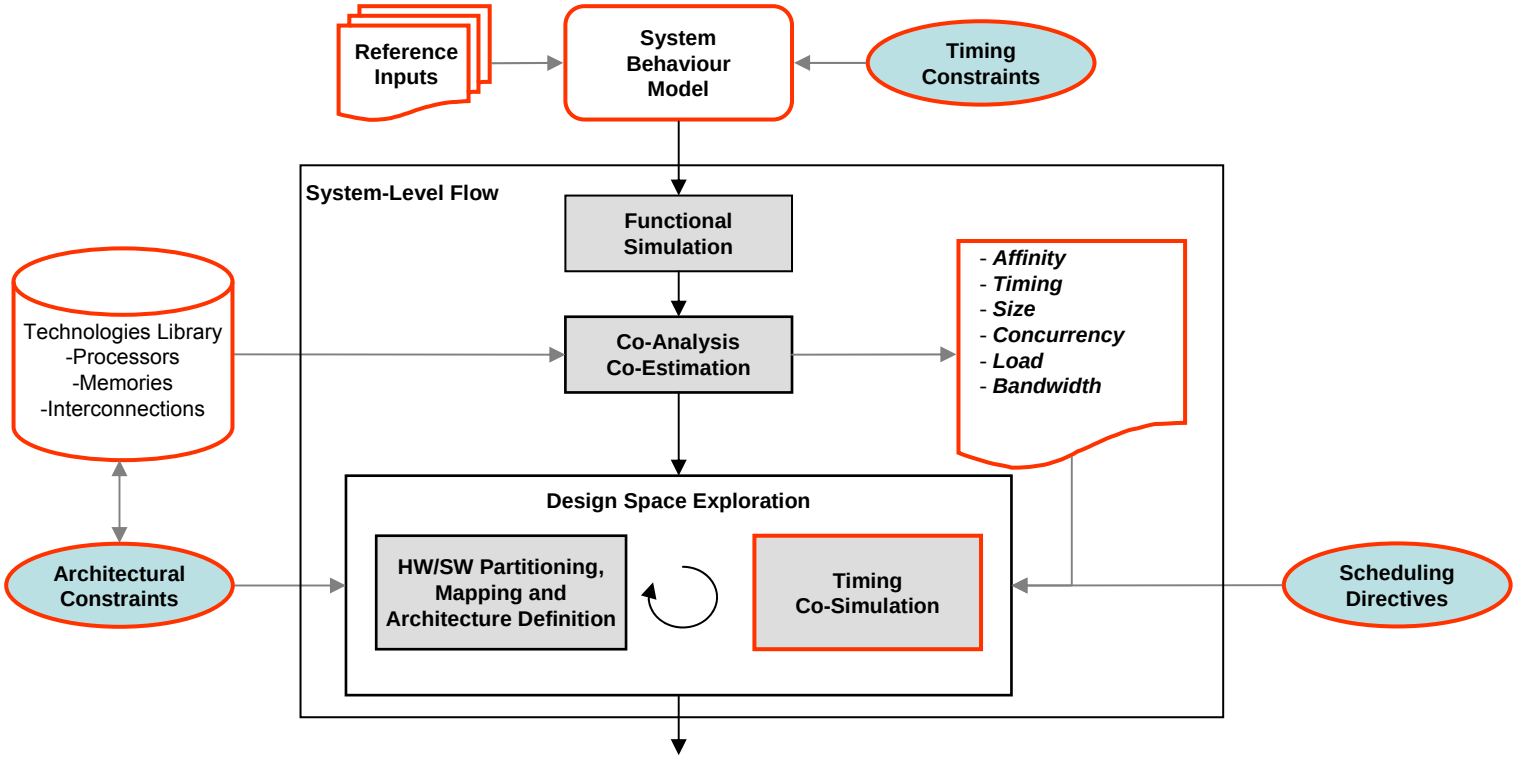
The Proposed Methodology

Design Space Exploration

Timing Co-Simulation

Design Space Exploration

Timing Co-Simulation



Design Space Exploration

- Timing Co-Simulation
  - The timing co-simulation activity considers the suggested HPDS (i.e. architecture and mapping) and all the relevant info previously collected to check if T is going to be satisfied
    - Scheduling Directives
      - Additionally, the designer can select a scheduling policy to be used
        - » e.g. round-robin, priority-based (if any), etc.
  - Currently based on standard SystemC kernel integrated with specific extensions

The Proposed Methodology

Design Space Exploration

Iterations

Design Space Exploration

- Iterations
  - If the proposed mapping/architecture doesn't satisfy T, the designer have to perform again the design space exploration
    - by changing scheduling directives
    - by changing some parameters in DSE heuristics
    - by changing architectural constraints
  - If no solutions are still found the designer have to perform other changes in the previous steps
    - by modifying the SBM
      - in order to apply semantically equivalent transformations to better show relevant features (e.g. concurrency or affinity) that the methodology could exploit
    - by modifying elements in TL or by relaxing T
      - **This means that T is not feasible with the selected technologies!**

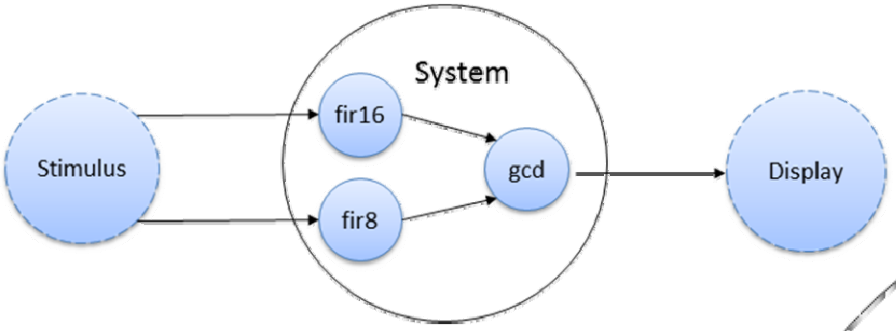
The Proposed Methodology

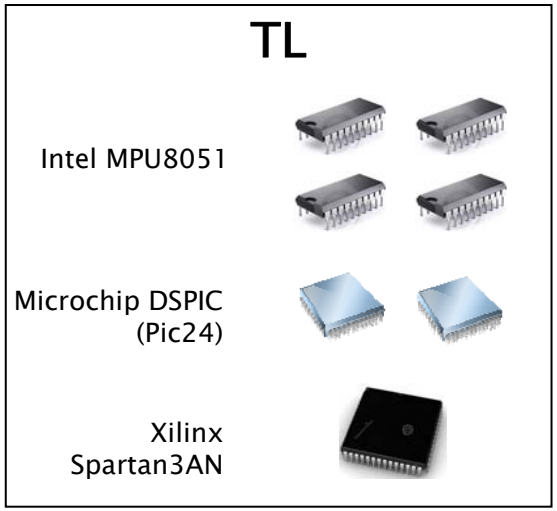
Design Space Exploration

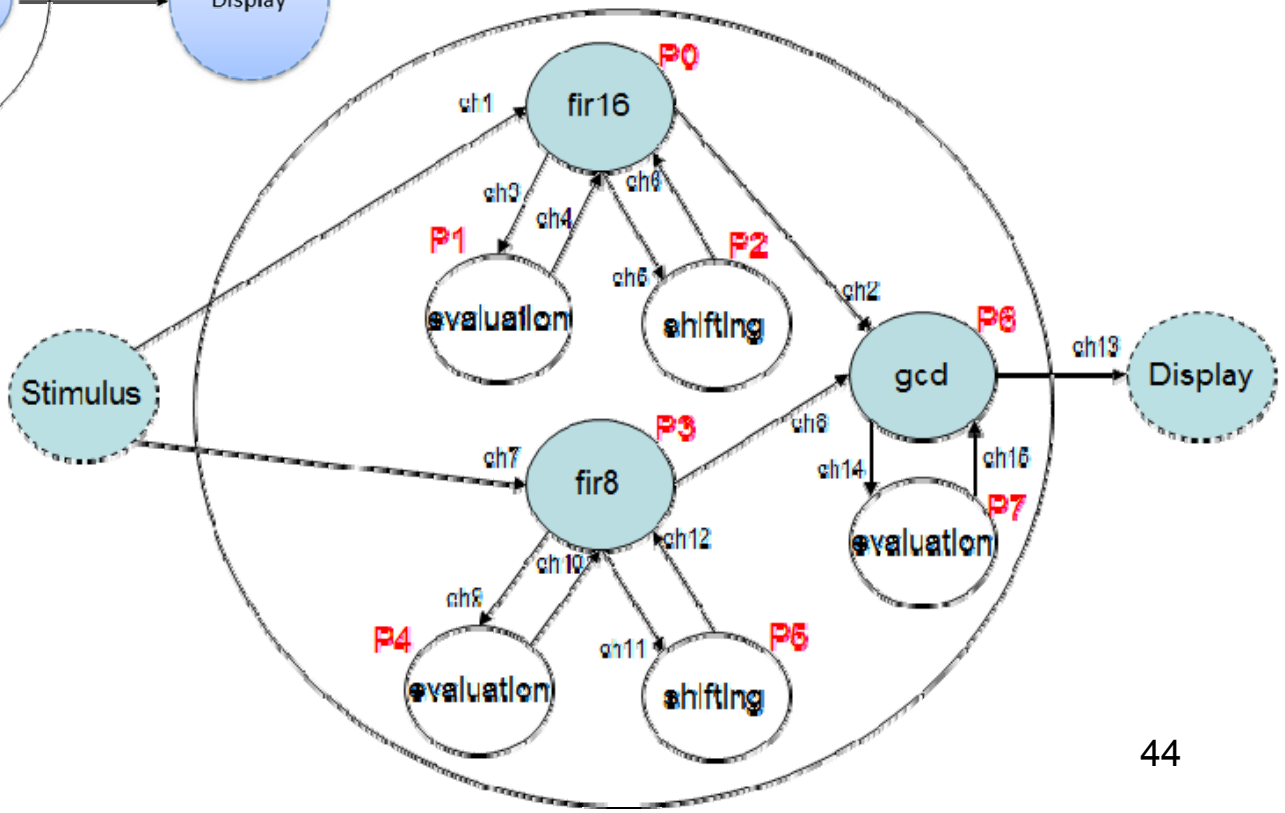
Example

Design Space Exploration

- Example







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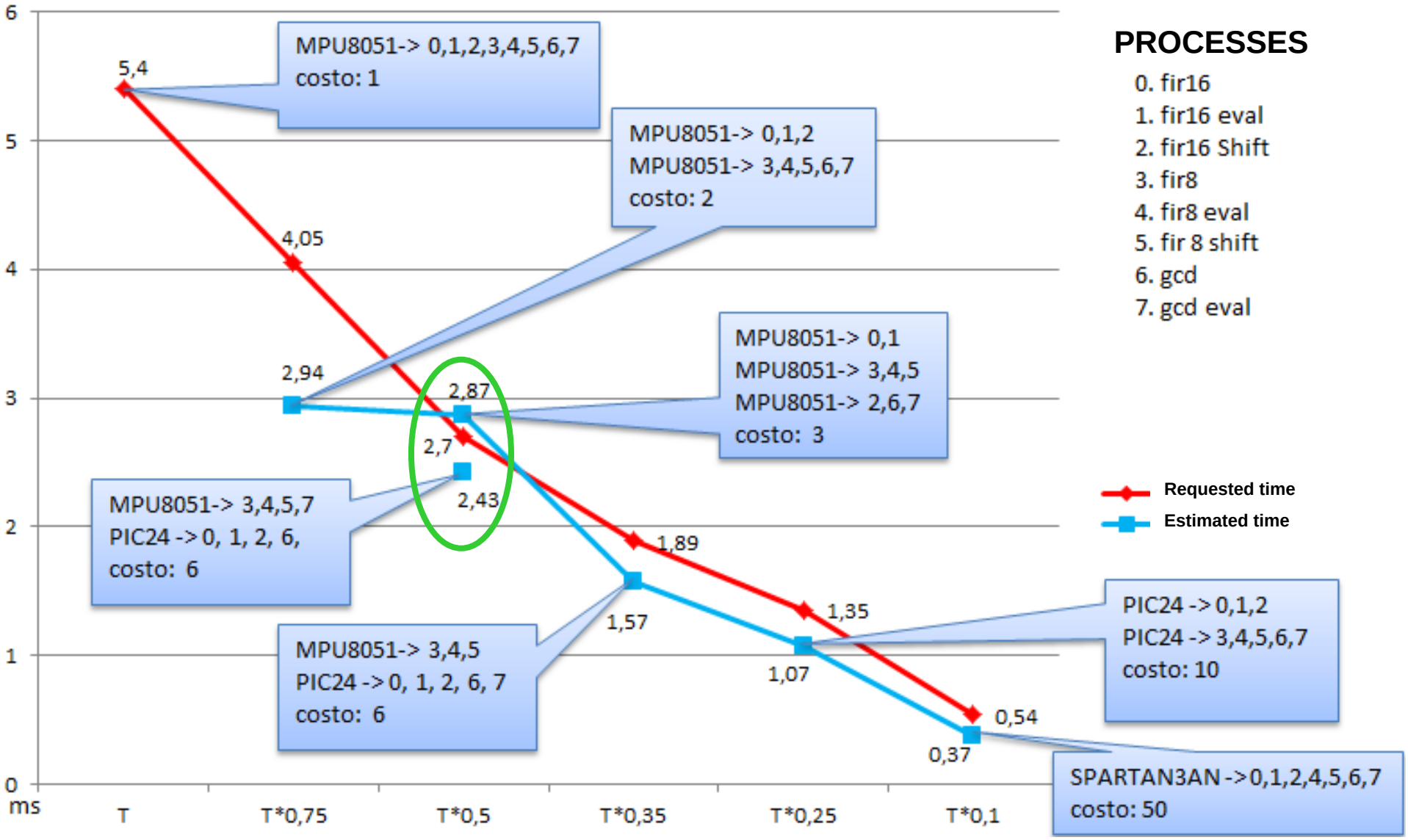

The Proposed Methodology

Main References

Main References

- L. Pomante, D. Sciuto, F. Salice, W. Fornaciari, C. Brandolese. “Affinity-Driven System Design Exploration for Heterogeneous Multiprocessor SoC”, *IEEE Transactions on Computers*, vol. 55, no. 5, May 2006.
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