Device notifications and improved efficiency

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LEADING
COLLABORATION
IN THE ARM
ECOSYSTEM

ARM DynamIQ

- ARM DynamIQ technology
  - Different microarchitectures can exist within same cluster.
  - Share the same last level of cache (L3), i.e. DSU (DynamIQ shared unit).
  - Different compute capacity and frequency domains for big and LITTLE.

- All the entities can do DVFS: big, LITTLE and DSU.
- Same voltage domain possible for DSU and big or/and LITTLE CPUs.
- DSU controls the cache bandwidth available to CPUs.
- DSU bandwidth configured based on requirements from CPUs.

Problem statement (example)

- LITTLE CPUs and DSU share voltage domain.
- Freq ranges: LITTLE - 500 to 1800 MHz, big - 900 to 2300 MHz.
- LITTLE CPU requests 500 MHz, voltage domain programmed accordingly.
- Big CPU programmed for 2300 MHz
  - DSU must provide more bandwidth, requests higher voltage for voltage domain.
- The new selected voltage of the shared domain can support 1800 MHz for LITTLE.
- LITTLE running at 500 MHz while it can run at 1800 MHz efficiently.
  - Power is proportional to V^2.F.
  - A 10% increase in voltage (at same freq) would mean 21% increase in power.
  - Finish work early and go to deep idle state, be more power efficient.
- There can be more issues like this among devices sharing voltage domains.

Proposed solution

- Enhance performance state feature of genpd.
- Represent the shared voltage domain as a genpd with performance states.
- Program the highest requested state from DSU and little CPUs.
- Add a new helper in genpd to register device notifier for performance state updates.
- Notifiers will be called if genpd programmed for higher state than requested by device.
  - Two states per device: Requested state and effective state.
- Call the notifier again before reducing performance state.
- How to support these new notifiers ?
  - A new genpd helper ?
  - A new helper in struct dev_pm_ops ?
    - It only handles suspend/resume currently.

Thank You

For further information: www.linaro.org