









Simplifying assumptions

- Single processor
- Homogeneous task sets
- Fully preemptive tasks
- Simultaneous activations
- No precedence constraints
- No resource constraints











It selects the ready task with the shortest computation time.

- Static (C_i is a constant parameter)
- It can be used on line or off-line
- Can be preemptive or non preemptive
- It minimizes the average response time













































- Each task is <u>statically allocated</u> in a slot in order to meet the desired request rate.
- The execution in each slot is activated by a timer.

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Cycling Scheduling		
ini	<pre>tialize_timer(MINOR);</pre>	// interrupt every 25 ms
whi	<pre>le (1) { sync(); function_A(); function_B();</pre>	// block until interrupt
	<pre>sync(); function_A(); function_C();</pre>	// block until interrupt
	<pre>sync(); function_A(); function_B();</pre>	// block until interrupt
}	<pre>sync(); function_A();</pre>	// block until interrupt

Advantages

- Simple implementation (no RTOS is required).
- Low run-time overhead.
- All tasks run with very low jitter.

Disadvantages

- It is not robust during overloads.
- It is difficult to expand the schedule.
- It is not easy to handle aperiodic activities.

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How can we verify feasibility?

• Each task uses the processor for a fraction of time:

$$U_i = \frac{C_i}{T_i}$$

• Hence the total processor utilization is:

$$U_p = \sum_{i=1}^n \frac{C_i}{T_i}$$

• U_p is a measure of the **processor load**.

Section
Bounding complexity
• Moreover we note that:
$$g(0, L) \le G(0, L)$$

 $G(0, L) = \sum_{i=1}^{n} \left(\frac{L+T_i - D_i}{T_i} \right) C_i$
 $= \sum_{i=1}^{n} L \frac{C_i}{T_i} + \sum_{i=1}^{n} (T_i - D_i) \frac{C_i}{T_i}$
 $= LU + \sum_{i=1}^{n} (T_i - D_i) U_i$

